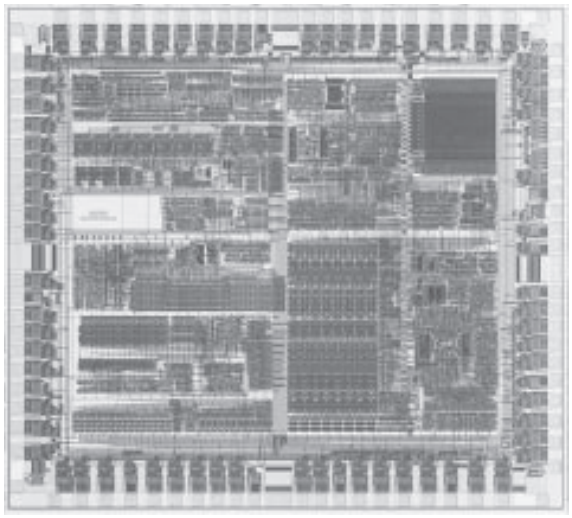
PRELIMINARY

80C186EA/80C188EA AND 80L186EA/80L188EA 16-BIT HIGH-INTEGRATION EMBEDDED PROCESSORS

- 80C186 Upgrade for Power Critical Applications
- Fully Static Operation
- True CMOS Inputs and Outputs

- Integrated Feature Set
  - Static 186 CPU Core
  - Power Save, Idle and Powerdown Modes
  - Clock Generator
  - 2 Independent DMA Channels
  - 3 Programmable 16-Bit Timers
  - Dynamic RAM Refresh Control Unit
  - Programmable Memory and Peripheral Chip Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
  - System-Level Testing Support (High Impedance Test Mode)
- Speed Versions Available (5V):
  - 25 MHz (80C186EA25/80C188EA25)
  - 20 MHz (80C186EA20/80C188EA20)
  - 13 MHz (80C186EA13/80C188EA13)
- Speed Versions Available (3V):
  - 13 MHz (80L186EA13/80L188EA13)
  - 8 MHz (80L186EA8/80L188EA8)
- Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O
- Supports 80C187 Numeric Coprocessor Interface (80C186EA only)
- Available in the Following Packages:
  - 68-Pin Plastic Leaded Chip Carrier (PLCC)
  - 80-Pin EIAJ Quad Flat Pack (QFP)
  - 80-Pin Shrink Quad Flat Pack (SQFP)
- Available in Extended Temperature Range (−40°C to +85°C)

The 80C186EA is a CHMOS high integration embedded microprocessor. The 80C186EA includes all of the features of an ''Enhanced Mode'' 80C186 while adding the additional capabilities of Idle and Powerdown Modes. In Numerics Mode, the 80C186EA interfaces directly with an 80C187 Numerics Coprocessor.



272432–1

October 1995 Order Number: 272432-003

MCS-86	**8086 – 8088 – 80C86 – 80C88**

Ceibo In-Circuit Emulator Supporting MCS-86:	**DS-186** **http://ceibo.com/eng/products/ds186.shtml**

80C186EA/80C188EA AND 80L186EA/80L188EA 16-Bit High Integration Embedded Processor

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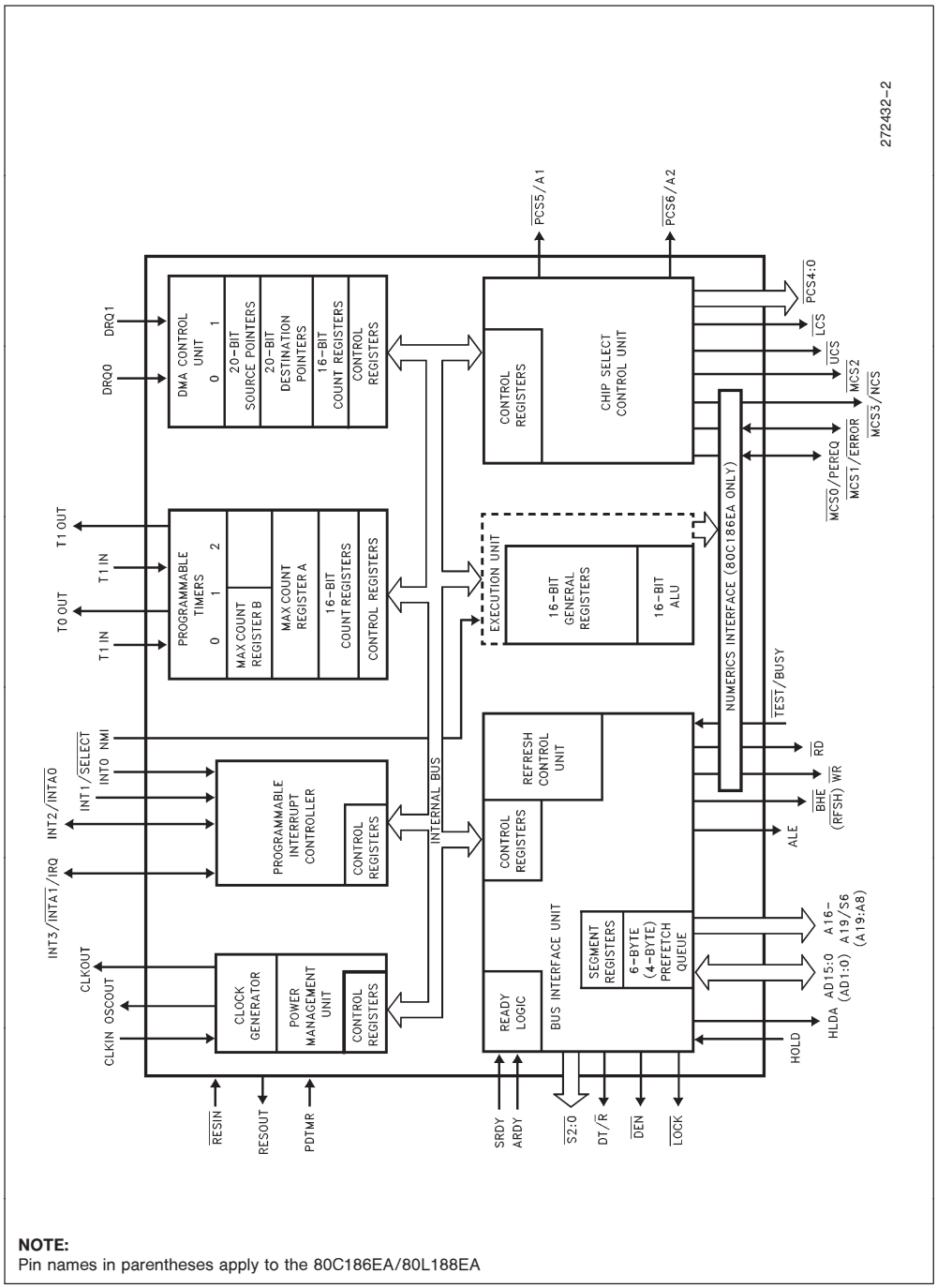


NOTE:
Pin names in parentheses apply to the 80C186EA/80L188EA

Figure 1. 80C186EA/80C188EA Block Diagram

INTRODUCTION

Unless specifically noted, all references to the 80C186EA apply to the 80C188EA, 80L186EA, and 80L188EA. References to pins that differ between the 80C186EA/80L186EA and the 80C188EA/80L188EA are given in parentheses. The ''L'' in the part number denotes low voltage operation. Physically and functionally, the ''C'' and ''L'' devices are identical.

The 80C186EA is the second product in a new generation of low-power, high-integration microprocessors. It enhances the existing 80C186XL family by offering new features and operating modes. The 80C186EA is object code compatible with the 80C186XL embedded processor.

The 80L186EA is the 3V version of the 80C186EA. The 80L186EA is functionally identical to the 80C186EA embedded processor. Current 80C186EA customers can easily upgrade their designs to use the 80L186EA and benefit from the reduced power consumption inherent in 3V operation.

The feature set of the 80C186EA/80L186EA meets the needs of low-power, space-critical applications. Low-power applications benefit from the static design of the CPU core and the integrated peripherals as well as low voltage operation. Minimum current consumption is achieved by providing a Powerdown Mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space-critical applications benefit from the integration of commonly used system peripherals. Two flexible DMA channels perform CPU-independent data transfers. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 128 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters round out the feature set of the 80C186EA.

Figure 1 shows a block diagram of the 80C186EA/80C188EA. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions, and static operation. The Bus Interface Unit (BIU) is the same as that found on the original 80C186 family products. An independent internal bus is used to allow communication between the BIU and internal peripherals.

80C186EA CORE ARCHITECTURE

Bus Interface Unit

The 80C186EA core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. SRDY and ARDY input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the mulitplexed address/data bus.

Clock Generator

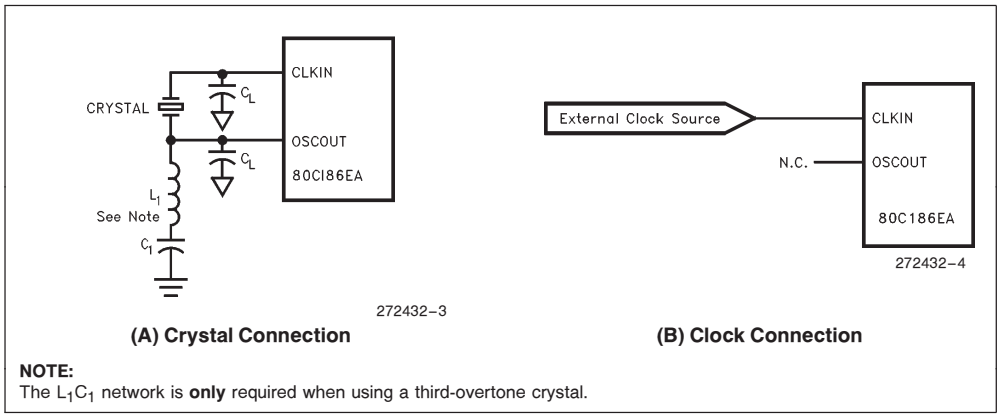
The processor provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ± 2 pF
Drive Level:	2 mW max



(A) Crystal Connection **(B) Clock Connection**

NOTE:
The L_1C_1 network is **only** required when using a third-overtone crystal.

Figure 2. Clock Configurations

80C186EA PERIPHERAL ARCHITECTURE

The 80C186EA has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or DMA channels).

The list of integrated peripherals include:

- 4-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel DMA Unit
- 13-Output Chip-Select Unit
- Refresh Control Unit
- Power Management logic

The registers associated with each integrated periheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 byte address boundary.

Figure 3 provides a list of the registers associated with the PCB when the processor's Interrupt Control Unit is in Master Mode. In Slave Mode, the definitions of some registers change. Figure 4 provides register definitions specific to Slave Mode.

Interrupt Control Unit

The 80C186EA can receive interrupts from a number of sources, both internal and external. The Interrupt Control Unit (ICU) serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and DMA channels. External interrupt sources come from the four input pins INT3:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the timers only have one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer Unit.

Timer/Counter Unit

The 80C186EA Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts, etc.

PCB Offset	Function
00H	Reserved
02H	Reserved
04H	Reserved
06H	Reserved
08H	Reserved
0AH	Reserved
0CH	Reserved
0EH	Reserved
10H	Reserved
12H	Reserved
14H	Reserved
16H	Reserved
18H	Reserved
1AH	Reserved
1CH	Reserved
1EH	Reserved
20H	Reserved
22H	End of Interrupt
24H	Poll
26H	Poll Status
28H	Interrupt Mask
2AH	Priority Mask
2CH	In-Service
2EH	Interrupt Request
30H	Interrupt Status
32H	Timer Control
34H	DMA0 Int. Control
36H	DMA1 Int. Control
38H	INT0 Control
3AH	INT1 Control
3CH	INT2 Control
3EH	INT3 Control

PCB Offset	Function
40H	Reserved
42H	Reserved
44H	Reserved
46H	Reserved
48H	Reserved
4AH	Reserved
4CH	Reserved
4EH	Reserved
50H	Timer 0 Count
52H	Timer 0 Compare A
54H	Timer 0 Compare B
56H	Timer 0 Control
58H	Timer 1 Count
5AH	Timer 1 Compare A
5CH	Timer 1 Compare B
5EH	Timer 1 Control
60H	Timer 2 Count
62H	Timer 2 Compare
64H	Reserved
66H	Timer 2 Control
68H	Reserved
6AH	Reserved
6CH	Reserved
6EH	Reserved
70H	Reserved
72H	Reserved
74H	Reserved
76H	Reserved
78H	Reserved
7AH	Reserved
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	Reserved
82H	Reserved
84H	Reserved
86H	Reserved
88H	Reserved
8AH	Reserved
8CH	Reserved
8EH	Reserved
90H	Reserved
92H	Reserved
94H	Reserved
96H	Reserved
98H	Reserved
9AH	Reserved
9CH	Reserved
9EH	Reserved
A0H	UMCS
A2H	LMCS
A4H	PACS
A6H	MMCS
A8H	MPCS
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Reserved
B2H	Reserved
B4H	Reserved
B6H	Reserved
B8H	Reserved
BAH	Reserved
BCH	Reserved
BEH	Reserved

PCB Offset	Function
C0H	DMA0 Src. Lo
C2H	DMA0 Src. Hi
C4H	DMA0 Dest. Lo
C6H	DMA0 Dest. Hi
C8H	DMA0 Count
CAH	DMA0 Control
CCH	Reserved
CEH	Reserved
D0H	DMA1 Src. Lo
D2H	DMA1 Src. Hi
D4H	DMA1 Dest. Lo
D6H	DMA1 Dest. Hi
D8H	DMA1 Count
DAH	DMA1 Control
DCH	Reserved
DEH	Reserved
E0H	Refresh Base
E2H	Refresh Time
E4H	Refresh Control
E6H	Reserved
E8H	Reserved
EAH	Reserved
ECH	Reserved
EEH	Reserved
F0H	Power-Save
F2H	Power Control
F4H	Reserved
F6H	Step ID
F8H	Reserved
FAH	Reserved
FCH	Reserved
FEH	Relocation

Figure 3. Peripheral Control Block Registers

PCB Offset	Function
20H	Interrupt Vector
22H	Specific EOI
24H	Reserved
26H	Reserved
28H	Interrupt Mask
2AH	Priority Mask
2C	In-Service
2E	Interrupt Request
30	Interrupt Status
32	TMR0 Interrupt Control
34	DMA0 Interrupt Control
36	DMA1 Interrupt Control
38	TMR1 Interrupt Control
3A	TMR2 Interrupt Control
3C	Reserved
3E	Reserved

Figure 4. 80C186EA Slave Mode Peripheral Control Block Registers

DMA Control Unit

The 80C186EA DMA Contol Unit provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O space in any combination: memory to memory, memory to I/O, I/O to I/O or I/O to memory. Data can be transferred either in bytes or words. Transfers may proceed to or from either even or odd addresses, but even-aligned word transfers proceed at a faster rate. Each data transfer consumes two bus cycles (a minimum of eight clocks), one cycle to fetch data and the other to store data. The chip-select/ready logic may be programmed to point to the memory or I/O space subject to DMA transfers in order to provide hardware chip select lines. DMA cycles run at higher priority than general processor execution cycles.

Chip-Select Unit

The 80C186EA Chip-Select Unit integrates logic which provides up to 13 programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically terminate a bus cycle independent of the condition of the SRDY and ARDY input pins. The chip-select lines are available for all memory and I/O bus cycles, whether they are generated by the CPU, the DMA unit, or the Refresh Control Unit.

Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 9-bit address generator is maintained by the RCU with the address presented on the A9:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

Power Management

The 80C186EA has three operational modes to control the power consumption of the device. They are Power Save Mode, Idle Mode, and Powerdown Mode.

Power Save Mode divides the processor clock by a programmable value to take advantage of the fact that current is linearly proportional to frequency. An unmasked interrupt, NMI, or reset will cause the 80C186EA to exit Power Save Mode.

Idle Mode freezes the clocks of the Execution Unit and the Bus Interface Unit at a logic zero state while all peripherals operate normally.

Powerdown Mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to transistor leakage only.

80C187 Interface (80C186EA Only)

The 80C187 Numerics Coprocessor may be used to extend the 80C186EA instruction set to include floating point and advanced integer instructions. Connecting the 80C186EA RESOUT and $\overline{TEST}$/BUSY pins to the 80C187 enables Numerics Mode operation. In Numerics Mode, three of the four Mid-Range Chip Select ($\overline{MCS}$) pins become handshaking pins for the interface. The exchange of data and control information proceeds through four dedicated I/O ports.

If an 80C187 is not present, the 80C186EA configures itself for regular operation at reset.

NOTE:
The 80C187 is not specified for 3V operation and therefore does not interface directly to the 80L186EA.

ONCE Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186EA has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for ''ON Circuit Emulation''. The ONCE mode is selected by forcing the $\overline{UCS}$ and $\overline{LCS}$ pins LOW (0) during a processor reset (these pins are weakly held to a HIGH (1) level) while $\overline{RESIN}$ is active.

DIFFERENCES BETWEEN THE 80C186XL AND THE 80C186EA

The 80C186EA is intended as a direct functional upgrade for 80C186XL designs. In many cases, it will be possible to replace an existing 80C186XL with little or no hardware redesign. The following sections describe differences in pinout, operating modes, and AC and DC specifications to keep in mind.

Pinout Compatibility

The 80C186EA requires a PDTMR pin to time the processor's exit from Powerdown Mode. The original pin arrangement for the 80C186XL in the PLCC package did not have any spare leads to use for PDTMR, so the DT/$\overline{R}$ pin was sacrificed. The arrangement of all the other leads in the 68-lead PLCC is identical between the 80C186XL and the 80C186EA. DT/$\overline{R}$ may be synthesized by latching the $\overline{S1}$ status output. Therefore, upgrading a PLCC 80C186XL to PLCC 80C186EA is straightforward.

The 80-lead QFP (EIAJ) pinouts are different between the 80C186XL and the 80C186EA. In addition to the PDTMR pin, the 80C186EA has more power and ground pins and the overall arrangement of pins was shifted. A new circuit board layout for the 80C186EA is required.

Operating Modes

The 80C186XL has two operating modes, Compatible and Enhanced. Compatible Mode is a pin-to-pin replacement for the NMOS 80186, except for numerics coprocessing. In Enhanced Mode, the processor has a Refresh Control Unit, the Power-Save feature and an interface to the 80C187 Numerics Coprocessor. The $\overline{MCS0}$, $\overline{MCS1}$, and $\overline{MCS3}$ pins change their functions to constitute handshaking pins for the 80C187.

The 80C186EA allows all non-80C187 users to use all the $\overline{MCS}$ pins for chip-selects. In regular operation, all 80C186EA features (including those of the Enhanced Mode 80C186) are present except for the interface to the 80C187. Numerics Mode disables the three chip-select pins and reconfigures them for connection to the 80C187.

TTL vs CMOS Inputs

The inputs of the 80C186EA are rated for CMOS switching levels for improved noise immunity, but the 80C186XL inputs are rated for TTL switching levels. In particular, the 80C186EA requires a minimum V_{IH} of 3.5V to recognize a logic one while the 80C186XL requires a minimum V_{IH} of only 1.9V (assuming 5.0V operation). The solution is to drive the 80C186EA with true CMOS devices, such as those from the HC and AC logic families, or to use pullup resistors where the added current draw is not a problem.

Timing Specifications

80C186EA timing relationships are expressed in a simplified format over the 80C186XL. The AC performance of an 80C186EA at a specified frequency will be very close to that of an 80C186XL at the same frequency. Check the timings applicable to your design prior to replacing the 80C186XL.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80C186EA in the Plastic Leaded Chip Carrier (PLCC) package, Shrink Quad Flat Pack (SQFP), and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

With the extended temperature range operational characteristics are guaranteed over a temperature range corresponding to −40°C to +85°C ambient. Package types are identified by a two-letter prefix to the part number. The prefixes are listed in Table 1.

Table 1. Prefix Identification

Prefix	Note	Package Type	Temperature Range
TN		PLCC	Extended
TS		QFP (EIAJ)	Extended
SB	1	SQFP	Extended/Commercial
N	1	PLCC	Commercial
S	1	QFP (EIAJ)	Commercial

NOTE:
1. The 25 MHz version is only available in commercial temperature range corresponding to 0°C to +70°C ambient.

Pin Descriptions

Each pin or logical set of pins is described in Table 3. There are three columns for each entry in the Pin Description Table.

The **Pin Name** column contains a mnemonic that describes the pin function. Negation of the signal name (for example, $\overline{\text{RESIN}}$) denotes a signal that is active low.

The **Pin Type** column contains two kinds of information. The first symbol indicates whether a pin is power (P), ground (G), input only (I), output only (O) or input/output (I/O). Some pins have multiplexed functions (for example, A19/S6). Additional symbols indicate additional characteristics for each pin. Table 3 lists all the possible symbols for this column.

The **Input Type** column indicates the type of input (asynchronous or synchronous).

Asynchronous pins require that setup and hold times be met only in order to guarantee *recognition* at a particular clock edge. Synchronous pins require that setup and hold times be met to guarantee proper *operation.* For example, missing the setup or hold time for the SRDY pin (a synchronous input) will result in a system failure or lockup. Input pins may also be edge- or level-sensitive. The possible characteristics for input pins are S(E), S(L), A(E) and A(L).

The **Output States** column indicates the output state as a function of the device operating mode. Output states are dependent upon the current activity of the processor. There are four operational states that are different from regular operation: bus hold, reset, Idle Mode and Powerdown Mode. Appropriate characteristics for these states are also indicated in this column, with the legend for all possible characteristics in Table 2.

The **Pin Description** column contains a text description of each pin.

As an example, consider AD15:0. I/O signifies the pins are bidirectional. S(L) signifies that the input function is synchronous and level-sensitive. H(Z) signifies that, as outputs, the pins are high-impedance upon acknowledgement of bus hold. R(Z) signifies that the pins float during reset. P(X) signifies that the pins retain their states during Powerdown Mode.

Table 2. Pin Description Nomenclature

Symbol	Description
P	Power Pin (Apply $+V_{CC}$ Voltage)
G	Ground (Connect to V_{SS})
I	Input Only Pin
O	Output Only Pin
I/O	Input/Output Pin
S(E)	Synchronous, Edge Sensitive
S(L)	Synchronous, Level Sensitive
A(E)	Asynchronous, Edge Sensitive
A(L)	Asynchronous, Level Sensitive
H(1)	Output Driven to V_{CC} during Bus Hold
H(0)	Output Driven to V_{SS} during Bus Hold
H(Z)	Output Floats during Bus Hold
H(Q)	Output Remains Active during Bus Hold
H(X)	Output Retains Current State during Bus Hold
R(WH)	Output Weakly Held at V_{CC} during Reset
R(1)	Output Driven to V_{CC} during Reset
R(0)	Output Driven to V_{SS} during Reset
R(Z)	Output Floats during Reset
R(Q)	Output Remains Active during Reset
R(X)	Output Retains Current State during Reset
I(1)	Output Driven to V_{CC} during Idle Mode
I(0)	Output Driven to V_{SS} during Idle Mode
I(Z)	Output Floats during Idle Mode
I(Q)	Output Remains Active during Idle Mode
I(X)	Output Retains Current State during Idle Mode
P(1)	Output Driven to V_{CC} during Powerdown Mode
P(0)	Output Driven to V_{SS} during Powerdown Mode
P(Z)	Output Floats during Powerdown Mode
P(Q)	Output Remains Active during Powerdown Mode
P(X)	Output Retains Current State during Powerdown Mode

Table 3. Pin Descriptions

Pin Name	Pin Type	Input Type	Output States	Description
V_{CC}	P			**POWER** connections consist of six pins which must be shorted externally to a V_{CC} board plane.
V_{SS}	G			**GROUND** connections consist of five pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I	A(E)		**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O		H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O		H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I	A(L)		**RESet IN** causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the processor begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O		H(0) R(1) P(0)	**RESet OUTput** that indicates the processor is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active. When tied to the $\overline{\text{TEST}}$/BUSY pin, RESOUT forces the 80C186EA into Numerics Mode.
PDTMR	I/O	A(L)	H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the processor waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I	A(E)		**Non-Maskable Interrupt** input causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$/BUSY ($\overline{\text{TEST}}$)	I	A(E)		**$\overline{\text{TEST}}$/BUSY** is sampled upon reset to determine whether the 80C186EA is to enter Numerics Mode. In regular operation, the pin is **$\overline{\text{TEST}}$.** $\overline{\text{TEST}}$ is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low). In Numerics Mode, the pin is **BUSY**. BUSY notifies the 80C186EA of 80C187 Numerics Coprocessor activity.
AD15:0 (AD7:0)	I/O	S(L)	H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 (0 through 7 on the 8-bit bus versions) are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.

NOTE:
Pin names in parentheses apply to the 80C188EA and 80L188EA.

Table 3. Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Description
A18:16 A19/S6–A16 (A19–A8)	O		H(Z) R(Z) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. A18:16 are driven to a logic 0 during the data phase of the bus cycle. On the 8-bit bus versions, A15–A8 provide valid address information for the entire bus cycle. Also during the data phase, S6 is driven to a logic 0 to indicate a CPU-initiated bus cycle or logic 1 to indicate a DMA-initiated bus cycle or a refresh cycle.
$\overline{S2:0}$	O		H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Processor HALT
1	0	0	Queue Instruction Fetch
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive (no bus activity)

ALE/QS0	O		H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle. In Queue Status Mode, QS0 provides queue status information along with QS1.
$\overline{BHE}$ ($\overline{RFSH}$)	O		H(Z) R(Z) P(X)	**Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding:

A0	$\overline{BHE}$	Encoding (For 80C186EA/80L186EA Only)
0	0	Word Transfer
0	1	Even Byte Transfer
1	0	Odd Byte Transfer
1	1	Refresh Operation

On the 80C188EA/80L188EA, $\overline{RFSH}$ is asserted low to indicate a Refresh bus cycle.

$\overline{RD}$/$\overline{QSMD}$	O		H(Z) R(WH) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus. Upon reset, this pin has an alternate function. As $\overline{QSMD}$, it enables **Queue Status Mode** when grounded. In Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide the following information about processor/instruction queue interaction:

QS1	QS0	Queue Operation
0	0	No Queue Operation
0	1	First Opcode Byte Fetched from the Queue
1	1	Subsequent Byte Fetched from the Queue
1	0	Empty the Queue

NOTE:
Pin names in parentheses apply to the 80C188EA and 80L188EA.

Table 3. Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Description
$\overline{WR}$/QS1	O		H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. In Queue Status Mode, QS1 provides queue status information along with QS0.
ARDY	I	A(L) S(L)		**Asychronous ReaDY** is an input to signal for the end of a bus cycle. ARDY is asynchronous on rising CLKOUT and synchronous on falling CLKOUT. ARDY or SRDY must be active to terminate any processor bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
SRDY	I	S(L)		**Synchronous ReaDY** is an input to signal for the end of a bus cycle. ARDY or SRDY must be active to terminate any processor bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
$\overline{DEN}$	O	H(Z) R(Z) P(1)		**Data ENable** output to control the enable of bidirectional transceivers when buffering a system. $\overline{DEN}$ is active only when data is to be transferred on the bus.
DT/$\overline{R}$	O		H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer in a buffered system. DT/$\overline{R}$ is only available on the QFP (EIAJ) package and the SQFP package.
$\overline{LOCK}$	O		H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The processor will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I	A(L)		**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The processor will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O		H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the processor has relinquished control of the local bus. When HLDA is asserted, the processor will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O		H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{LCS}$	O		H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.

NOTE:
Pin names in parentheses apply to the 80C188EA and 80L188EA.

Table 3. Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Description
MCS0/PEREQ MCS1/ERROR MCS2 MCS3/NCS	I/O	A(L)	H(1) R(1) P(1)	These pins provide a multiplexed function. If enabled, these pins normally comprise a block of **Mid-Range Chip Select** outputs which will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. In Numerics Mode (80C186EA only), three of the pins become handshaking pins for the 80C187. The **CoProcessor REQuest** input signals that a data transfer is pending. **ERROR** is an input which indicates that the previous numerics coprocessor operation resulted in an exception condition. An interrupt Type 16 is generated when ERROR is sampled active at the beginning of a numerics operation. **Numerics Coprocessor Select** is an output signal generated when the processor accesses the 80C187.
PCS4:0	O		H(1) R(1) P(1)	**Peripheral Chip Selects** go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
PCS5/A1 PCS6/A2	O		H(1)/H(X) R(1) P(1)	These pins provide a multiplexed function. As additional **Peripheral Chip Selects,** they go active whenever the address of a memory or I/O bus cycle is within the address limitations by the user. They may also be programmed to provide latched **Address** A2:1 signals.
T0OUT T1OUT	O		H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I	A(L) A(E)		**Timer INput** is used either as clock or control signals, depending on the timer mode selected.
DRQ0 DRQ1	I	A(L)		**DMA ReQuest** is asserted by an external request when it is prepared for a DMA transfer.
INT0 INT1/SELECT	I	A(E,L)		Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with INTA0 and INTA1 to interface with an external slave controller. INT1 becomes SELECT when the ICU is configured for Slave Mode.
INT2/INTA0 INT3/INTA1/IRQ	I/O	A(E,L)	H(1) R(Z) P(1)	These pins provide multiplexed functions. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an **INTerrupt Acknowledge** handshake signal to allow interrupt expansion. INT3/INTA1 becomes **IRQ** when the ICU is configured for Slave Mode.
N.C.				**No Connect.** For compatibility with future products, do not connect to these pins.

NOTE:
Pin names in parentheses apply to the 80C188EA and 80L188EA.

80C186EA PINOUT

Tables 4 and 5 list the 80C186EA pin names with package location for the 68-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 9 depicts the complete 80C186EA/80L186EA pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 6 and 7 list the 80C186EA pin names with package location for the 80-pin Quad Flat Pack (EIAJ) component. Figure 6 depicts the complete 80C186EA/80C188EA (EIAJ QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 8 and 9 list the 80C186EA/80C188EA pin names with package location for the 80-pin Shrink Quad Flat Pack (SQFP) component. Figure 7 depicts the complete 80C186EA/80C188EA (SQFP) as viewed from the top side of the component (i.e., contacts facing down).

Table 4. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
AD8 (A8)	16
AD9 (A9)	14
AD10 (A10)	12
AD11 (A11)	10
AD12 (A12)	7
AD13 (A13)	5
AD14 (A14)	3
AD15 (A15)	1
A16	68
A17	67
A18	66
A19/S6	65

Bus Control	
Name	**Location**
ALE/QS0	61
$\overline{BHE}$ ($\overline{RFSH}$)	64
$\overline{S0}$	52
$\overline{S1}$	53
$\overline{S2}$	54
$\overline{RD}$/$\overline{QSMD}$	62
$\overline{WR}$/QS1	63
ARDY	55
SRDY	49
$\overline{DEN}$	39
$\overline{LOCK}$	48
HOLD	50
HLDA	51

Power	
Name	**Location**
V_{SS}	26, 60
V_{CC}	9, 43

Processor Control	
Name	**Location**
$\overline{RESIN}$	24
RESOUT	57
CLKIN	59
OSCOUT	58
CLKOUT	56
$\overline{TEST}$/BUSY	47
PDTMR	40
NMI	46
INT0	45
INT1/SELECT	44
INT2/$\overline{INTA0}$	42
INT3/$\overline{INTA1}$/ IRQ	41

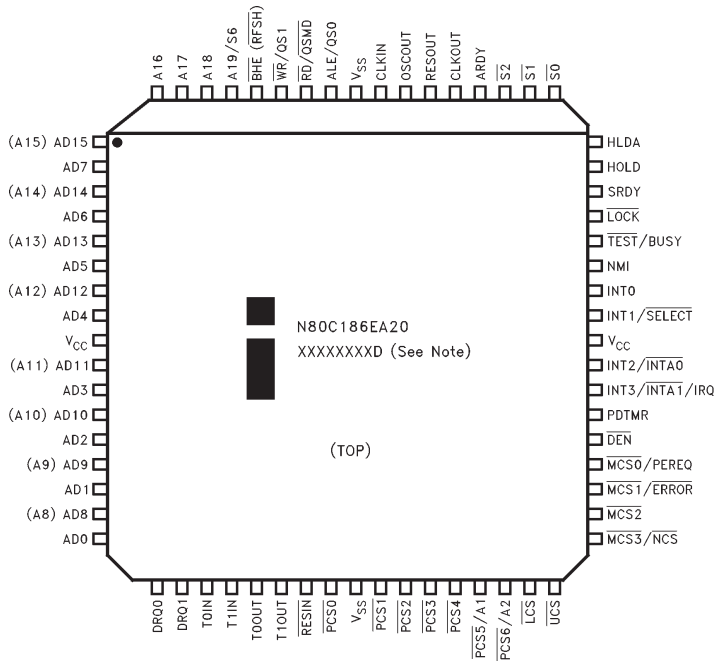
I/O	
Name	**Location**
$\overline{UCS}$	34
$\overline{LCS}$	33
$\overline{MCS0}$/PEREQ	38
$\overline{MCS1}$/$\overline{ERROR}$	37
$\overline{MCS2}$	36
$\overline{MCS3}$/$\overline{NCS}$	35
$\overline{PCS0}$	25
$\overline{PCS1}$	27
$\overline{PCS2}$	28
$\overline{PCS3}$	29
$\overline{PCS4}$	30
$\overline{PCS5}$/A1	31
$\overline{PCS6}$/A2	32
T0OUT	22
T0IN	20
T1OUT	23
T1IN	21
DRQ0	18
DRQ1	19

NOTE:
Pin names in parentheses apply to the 80C188EA/80L188EA.

Table 5. PLCC Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	AD15 (A15)	18	DRQ0	35	$\overline{MCS3}/\overline{NCS}$	52	$\overline{S0}$
2	AD7	19	DRQ1	36	$\overline{MCS2}$	53	$\overline{S1}$
3	AD14 (A14)	20	T0IN	37	$\overline{MCS1}/\overline{ERROR}$	54	$\overline{S2}$
4	AD6	21	T1IN	38	$\overline{MCS0}$/PEREQ	55	ARDY
5	AD13 (A13)	22	T0OUT	39	$\overline{DEN}$	56	CLKOUT
6	AD5	23	T1OUT	40	PDTMR	57	RESOUT
7	AD12 (A12)	24	$\overline{RESIN}$	41	INT3/$\overline{INTA1}$/	58	OSCOUT
8	AD4	25	$\overline{PCS0}$		IRQ	59	CLKIN
9	V_{CC}	26	V_{SS}	42	INT2/$\overline{INTA0}$	60	V_{SS}
10	AD11 (A11)	27	$\overline{PCS1}$	43	V_{CC}	61	ALE/QS0
11	AD3	28	$\overline{PCS2}$	44	INT1/SELECT	62	$\overline{RD}/\overline{QSMD}$
12	AD10 (A10)	29	$\overline{PCS3}$	45	INT0	63	$\overline{WR}$/QS1
13	AD2	30	$\overline{PCS4}$	46	NMI	64	$\overline{BHE}$ ($\overline{RFSH}$)
14	AD9 (A9)	31	$\overline{PCS5}$/A1	47	$\overline{TEST}$/BUSY	65	A19/S6
15	AD1	32	$\overline{PCS6}$/A2	48	LOCK	66	A18
16	AD8 (A8)	33	$\overline{LCS}$	49	SRDY	67	A17
17	AD0	34	$\overline{UCS}$	50	HOLD	68	A16
				51	HLDA		

NOTE:
Pin names in parentheses apply to the 80C186EA/80L188EA.



NOTES:
1. The nine-character alphanumeric code (XXXXXXXXD) underneath the product number is the Intel FPO number.
2. Pin names in parentheses apply to the 80C186EA/80L188EA.

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Figure 5. 68-Lead PLCC Pinout Diagram

Table 6. QFP (EIAJ) Pin Names with Package Location

Address/Data Bus		Bus Control		Processor Control		I/O	
Name	**Location**	**Name**	**Location**	**Name**	**Location**	**Name**	**Location**
AD0	64	ALE/QS0	10	$\overline{\text{RESIN}}$	55	$\overline{\text{UCS}}$	45
AD1	66	$\overline{\text{BHE}}$ ($\overline{\text{RFSH}}$)	7	RESOUT	18	$\overline{\text{LCS}}$	46
AD2	68	$\overline{\text{S0}}$	23	CLKIN	16	$\overline{\text{MCS0}}$/PEREQ	40
AD3	70	$\overline{\text{S1}}$	22	OSCOUT	17	$\overline{\text{MCS1}}$/$\overline{\text{ERROR}}$	41
AD4	74	$\overline{\text{S2}}$	21	CLKOUT	19	$\overline{\text{MCS2}}$	42
AD5	76	$\overline{\text{RD}}$/$\overline{\text{QSMD}}$	9	$\overline{\text{TEST}}$/BUSY	29	$\overline{\text{MCS3}}$/$\overline{\text{NCS}}$	43
AD6	78	$\overline{\text{WR}}$/QS1	8	PDTMR	38	$\overline{\text{PCS0}}$	54
AD7	80	ARDY	20	NMI	30	$\overline{\text{PCS1}}$	52
AD8 (A8)	65	SRDY	27	INT0	31	$\overline{\text{PCS2}}$	51
AD9 (A9)	67	DT/$\overline{\text{R}}$	37	INT1/$\overline{\text{SELECT}}$	32	$\overline{\text{PCS3}}$	50
AD10 (A10)	69	$\overline{\text{DEN}}$	39	INT2/$\overline{\text{INTA0}}$	35	$\overline{\text{PCS4}}$	49
AD11 (A11)	71	$\overline{\text{LOCK}}$	28	INT3/$\overline{\text{INTA1}}$/	36	$\overline{\text{PCS5}}$/A1	48
AD12 (A12)	75	HOLD	26	IRQ		$\overline{\text{PCS6}}$/A2	47
AD13 (A13)	77	HLDA	25	N.C.	11, 14, 15, 63	T0OUT	57
AD14 (A14)	79					T0IN	59
AD15 (A15)	1					T1OUT	56
A16	3					T1IN	58
A17	4					DRQ0	61
A18	5					DRQ1	60
A19/S6	6						

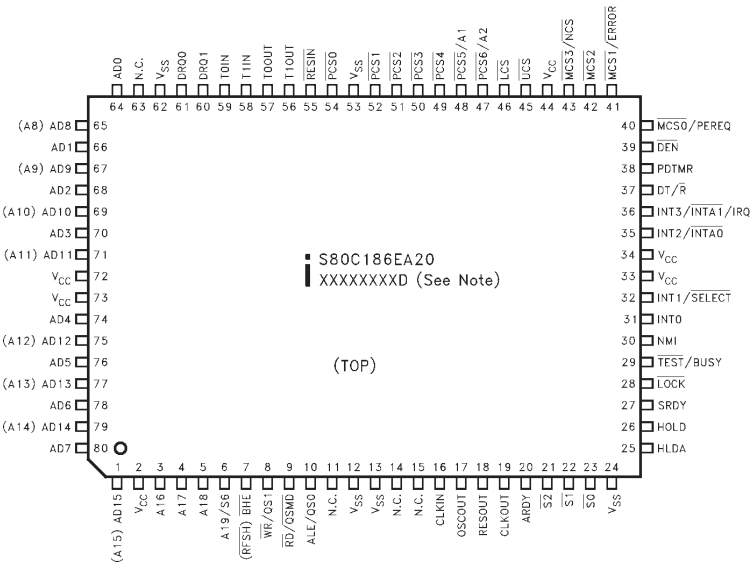
Power	
Name	**Location**
V_{SS}	12, 13, 24, 53,62
V_{CC}	2, 33, 34, 44, 72, 73

NOTE:
Pin names in parentheses apply to the 80C186EA/80L188EA.

Table 7. QFP (EIAJ) Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	AD15 (A15)	21	$\overline{S2}$	41	$\overline{MCS1}$/$\overline{ERROR}$	61	DRQ0
2	V_{CC}	22	$\overline{S1}$	42	$\overline{MCS2}$	62	V_{SS}
3	A16	23	$\overline{S0}$	43	$\overline{MCS3}$/$\overline{NCS}$	63	N.C.
4	A17	24	V_{SS}	44	V_{CC}	64	AD0
5	A18	25	HLDA	45	$\overline{UCS}$	65	AD8 (A8)
6	A19/S6	26	HOLD	46	$\overline{LCS}$	66	AD1
7	$\overline{BHE}$ ($\overline{RFSH}$)	27	SRDY	47	$\overline{PCS6}$/A2	67	AD9 (A9)
8	$\overline{WR}$/QS1	28	$\overline{LOCK}$	48	$\overline{PCS5}$/A1	68	AD2
9	$\overline{RD}$/$\overline{QSMD}$	29	$\overline{TEST}$/BUSY	49	$\overline{PCS4}$	69	AD10 (A10)
10	ALE/QS0	30	NMI	50	$\overline{PCS3}$	70	AD3
11	N.C.	31	INT0	51	$\overline{PCS2}$	71	AD11 (A11)
12	V_{SS}	32	INT1/$\overline{SELECT}$	52	$\overline{PCS1}$	72	V_{CC}
13	V_{SS}	33	V_{CC}	53	V_{SS}	73	V_{CC}
14	N.C.	34	V_{CC}	54	$\overline{PCS0}$	74	AD4
15	N.C.	35	INT2/$\overline{INTA0}$	55	$\overline{RESIN}$	75	AD12 (A12)
16	CLKIN	36	INT3/$\overline{INTA1}$/	56	T1OUT	76	AD5
17	OSCOUT		IRQ	57	T0OUT	77	AD13 (A13)
18	RESOUT	37	DT/$\overline{R}$	58	T1IN	78	AD6
19	CLKOUT	38	PDTMR	59	T0IN	79	AD14 (A14)
20	ARDY	39	$\overline{DEN}$	60	DRQ1	80	AD7
		40	$\overline{MCS0}$/PEREQ				

NOTE:
Pin names in parentheses apply to the 80C186EA/80L188EA.



NOTES:
1. The nine-character alphanumeric code (XXXXXXXXD) underneath the product number is the Intel FPO number.
2. Pin names in parentheses apply to the 80C186EA/80L188EA.

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Figure 6. Quad Flat Pack (EIAJ) Pinout Diagram

Table 8. SQFP Pin Functions with Package Location

AD Bus	
AD0	1
AD1	3
AD2	6
AD3	8
AD4	12
AD5	14
AD6	16
AD7	18
AD8 (A8)	2
AD9 (A9)	5
AD10 (A10)	7
AD11 (A11)	9
AD12 (A12)	13
AD13 (A13)	15
AD14 (A14)	17
AD15 (A15)	19
A16/S3	21
A17/S4	22
A18/S5	23
A19/S6	24

Bus Control	
ALE/QS0	29
$\overline{BHE}$/($\overline{RFSH}$)	26
$\overline{S0}$	40
$\overline{S1}$	39
$\overline{S2}$	38
$\overline{RD}$/$\overline{QSMD}$	28
$\overline{WR}$/QS1	27
ARDY	37
SRDY	44
$\overline{DEN}$	56
DT/$\overline{R}$	54
$\overline{LOCK}$	45
HOLD	43
HLDA	42

No Connection	
N.C.	4
N.C.	25
N.C.	35
N.C.	72

Processor Control	
$\overline{RESIN}$	73
RESOUT	34
CLKIN	32
OSCOUT	33
CLKOUT	36
$\overline{TEST}$/BUSY	46
NMI	47
INT0	48
INT1/$\overline{SELECT}$	49
INT2/$\overline{INTA0}$	52
INT3/$\overline{INTA1}$	53
PDTMR	55

Power and Ground	
V_{CC}	10
V_{CC}	11
V_{CC}	20
V_{CC}	50
V_{CC}	51
V_{CC}	61
V_{SS}	30
V_{SS}	31
V_{SS}	41
V_{SS}	70
V_{SS}	80

I/O	
$\overline{UCS}$	62
$\overline{LCS}$	63
$\overline{MCS0}$/PEREQ	57
$\overline{MCS1}$/$\overline{ERROR}$	58
$\overline{MCS2}$	59
$\overline{MCS3}$/$\overline{NPS}$	60
$\overline{PCS0}$	71
$\overline{PCS1}$	69
$\overline{PCS2}$	68
$\overline{PCS3}$	67
$\overline{PCS4}$	66
$\overline{PCS5}$/A1	65
$\overline{PCS6}$/A2	64
TMR IN 0	77
TMR IN 1	76
TMR OUT 0	75
TMR OUT 1	74
DRQ0	79
DRQ1	78

NOTE:
Pin names in parentheses apply to the 80C186EA/80L188EA.

Table 9. SQFP Pin Locations with Pin Names

1	AD0
2	AD8 (A8)
3	AD1
4	N.C.
5	AD9 (A9)
6	AD2
7	AD10 (A10)
8	AD3
9	AD11 (A11)
10	V_{CC}
11	V_{CC}
12	AD4
13	AD12 (A12)
14	AD5
15	AD13 (A13)
16	AD6
17	AD14 (A14)
18	AD7
19	AD15 (A15)
20	V_{CC}

21	A16/S3
22	A17/S4
23	A18/S5
24	A19/S6
25	N.C.
26	$\overline{BHE}$/($\overline{RFSH}$)
27	$\overline{WR}$/QS1
28	RD/$\overline{QSMD}$
29	ALE/QS0
30	V_{SS}
31	V_{SS}
32	X1
33	X2
34	RESET
35	N.C.
36	CLKOUT
37	ARDY
38	$\overline{S2}$
39	$\overline{S1}$
40	$\overline{S0}$

41	V_{SS}
42	HLDA
43	HOLD
44	SRDY
45	$\overline{LOCK}$
46	$\overline{TEST}$/BUSY
47	NMI
48	INT0
49	INT1/$\overline{SELECT}$
50	V_{CC}
51	V_{CC}
52	INT2/$\overline{INTA0}$
53	INT3/$\overline{INTA1}$
54	DT/$\overline{R}$
55	PDTMR
56	$\overline{DEN}$
57	$\overline{MCS0}$/PEREQ
58	$\overline{MCS1}$/$\overline{ERROR}$
59	$\overline{MCS2}$
60	$\overline{MCS3}$/$\overline{NPS}$

61	V_{CC}
62	$\overline{UCS}$
63	$\overline{LCS}$
64	$\overline{PCS6}$/A2
65	$\overline{PCS5}$/A1
66	$\overline{PCS4}$
67	$\overline{PCS3}$
68	$\overline{PCS2}$
69	$\overline{PCS1}$
70	V_{SS}
71	$\overline{PCS0}$
72	N.C.
73	$\overline{RES}$
74	TMR OUT 1
75	TMR OUT 0
76	TMR IN 1
77	TMR IN 0
78	DRQ1
79	DRQ0
80	V_{SS}

NOTE:
Pin names in parentheses apply to the 80C186EA/80L188EA.

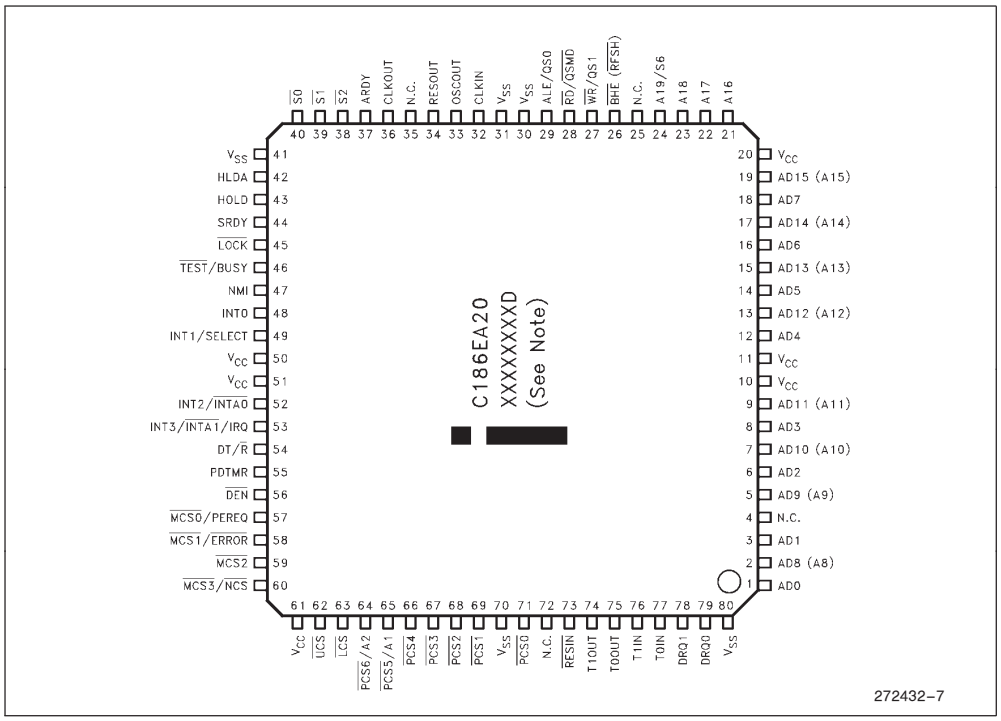


Figure 7. Shrink Quad Flat Pack (SQFP) Pinout Diagram

NOTES:
1. XXXXXXXXD indicates the Intel FPO number.
2. Pin names in parentheses apply to the 80C188EA.

PACKAGE THERMAL SPECIFICATIONS

The 80C186EA/80L186EA is specified for operation when T_C (the case temperature) is within the range of 0°C to 85°C (PLCC package) or 0°C to 106°C (QFP-EIAJ) package. T_C may be measured in any environment to determine whether the processor is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P \times \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 10.

P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5.5V.

Table 10. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	29	25	21	19	17	16.5
θ_{CA} (QFP)	66	63	60.5	59	58	57
θ_{CA} (SQFP)	70					

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Absolute Maximum Ratings*

Storage Temperature . . . . . −65°C to +150°C

Case Temperature under Bias . . . −65°C to +150°C

Supply Voltage with Respect to V_{SS} . . . . . −0.5V to +6.5V

Voltage on Other Pins with Respect to V_{SS} . . . . . −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C186EA based circuit board should contain separate power (V_{CC}) and ground (V_{SS}) planes. All V_{CC} and V_{SS} pins **must** be connected to the appropriate plane. Pins identified as "N.C." must not be connected in the system. Decoupling capacitors should be placed near the processor. The value and type of decoupling capacitors is application and board layout dependent. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Always connect any unused input pins to an appropriate signal level. In particular, unused interrupt pins (NMI, INT3:0) should be connected to V_{SS} to avoid unwanted interrupts. **Leave any unused output pin or any "N.C." pin unconnected.**

DC SPECIFICATIONS (80C186EA/80C188EA)

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Supply Voltage	4.5	5.5	V	
V_{IL}	Input Low Voltage for All Pins	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage for All Pins	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.30		V	
I_{IL1}	Input Leakage Current (except $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, $\overline{LOCK}$ and $\overline{TEST}$/BUSY)		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IL2}	Input Leakage Current ($\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$, $\overline{ERROR}$, $\overline{LOCK}$ and $\overline{TEST}$/BUSY	−275		μA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{OL}	Output Leakage Current		±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (RESET) 80C186EA25/80C188EA25 80C186EA20/80C188EA20 80C186EA13/80C188EA13		 105 90 65	 mA mA mA	(Notes 3, 5)
I_{ID}	Supply Current In Idle Mode 80C186EA25/80C188EA25 80C186EA20/80C188EA20 80C186EA13/80C188EA13		 90 70 46	 mA mA mA	(Note 5)
I_{PD}	Supply Current In Powerdown Mode 80C186EA25/80C188EA25 80C186EA20/80C188EA20 80C186EA13/80C188EA13		 100 100 100	 μA μA μA	(Note 5)
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 4)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz

NOTES:
1. $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, $\overline{LOCK}$ and $\overline{TEST}$/BUSY have internal pullups that are only activated during RESET. Loading these pins above I_{OL} = −275 μA will cause the processor to enter alternate modes of operation.
2. Output pins are floated using HOLD or ONCE Mode.
3. Measured at worst case temperature and V_{CC} with all outputs loaded as specified in the AC Test Conditions, and with the device in RESET ($\overline{RESIN}$ held low). RESET is worst case for I_{CC}.
4. Output capacitance is the capacitive load of a floating output pin.
5. Operating conditions for 25 MHz are 0°C to +70°C, V_{CC} = 5.0V ±10%.

DC SPECIFICATIONS (80L186EA/80L188EA)

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Supply Voltage	2.7	5.5	V	
V_{IL}	Input Low Voltage for All Pins	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage for All Pins	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA (min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −1 mA (min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.30		V	
I_{IL1}	Input Leakage Current (except $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$, $\overline{LOCK}$ and $\overline{TEST}$)		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IL2}	Input Leakage Current ($\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$ and $\overline{TEST}$)	−275		μA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{OL}	Output Leakage Current		±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC5}	Supply Current (RESET, 5.5V) 80L186EA-13 80L186EA-8		 65 40	 mA mA	 (Note 3) (Note 3)
I_{CC3}	Supply Current (RESET, 2.7V) 80L186EA-13 80L186EA-8		 34 20	 mA mA	 (Note 3) (Note 3)
I_{ID5}	Supply Current Idle (5.5V) 80L186EA-13 80L186EA-8		 46 28	 mA mA	
I_{ID5}	Supply Current Idle (2.7V) 80L186EA-13 80L186EA-8		 24 14	 mA mA	
I_{PD5}	Supply Current Powerdown (5.5V) 80L186EA-13 80L186EA-8		 100 100	 μA μA	
I_{PD3}	Supply Current Powerdown (2.7V) 80L186EA-13 80L186EA-8		 50 50	 μA μA	
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 4)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz

NOTES:
1. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$ and $\overline{TEST}$ have internal pullups that are only activated during RESET. Loading these pins above I_{OL} = −275 μA will cause the processor to enter alternate modes of operation.
2. Output pins are floated using HOLD or ONCE Mode.
3. Measured at worst case temperature and V_{CC} with all outputs loaded as specified in the AC Test Conditions, and with the device in RESET ($\overline{RESIN}$ held low).
4. Output capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the processor is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the 80C186EA would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 11). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 20 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.515 \times 20 \approx 49\ \text{mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132\ \mu$F is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Table 11. C_{DEV} Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.515	0.905	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.391	0.635	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80C186EA25/80C186EA20/80C186EA13

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
INPUT CLOCK		**25 MHz(12)**		**20 MHz**		**13 MHz**			
T_F	CLKIN Frequency	0	50	0	40	0	26	MHz	1
T_C	CLKIN Period	20	∞	25	∞	38.5	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	10	∞	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	10	∞	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	1	8	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	1	8	1	8	ns	1, 3
OUTPUT CLOCK									
T_{CD}	CLKIN to CLKOUT Delay	0	15	0	17	0	23	ns	1, 4
T	CLKOUT Period		$2T_C$		$2*T_C$		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5		(T/2) − 5		(T/2) − 5		ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5		(T/2) − 5		(T/2) − 5		ns	1
T_{PR}	CLKOUT Rise Time	1	6	1	6	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	1	6	1	6	ns	1, 5
OUTPUT DELAYS									
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, ($\overline{RFSH}$), $\overline{LOCK}$, A19:16	3	20	3	22	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	25	3	27	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$ ($\overline{RFSH}$), $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	20	3	22	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, AD15:0 (A15:8, AD7:0), $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	25	3	27	3	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	0	25	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0 (A15:8, AD7:0)	0	25	0	25	0	25	ns	1

AC SPECIFICATIONS (Continued)

AC Characteristics—80C186EA25/80C186EA20/80C186EA13

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
SYNCHRONOUS INPUTS		**25 MHz(12)**		**20 MHz**		**13 MHz**			
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	8		10		10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		3		3		ns	1, 9
T_{CLIS}	AD15:0 (AD7:0), ARDY, SRDY, DRQ1:0	10		10		10		ns	1, 10
T_{CLIH}	AD15:0 (AD7:0), ARDY, SRDY, DRQ1:0	3		3		3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$ (80C186EA Only)	10		10		10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$ (80C186EA Only)	3		3		3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	10		10		10		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		3		3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.
11. T_{CHOVS} applies to $\overline{BHE}$ ($\overline{RFSH}$) and A19:16 only after a HOLD release.
12. Operating conditions for 25 MHz are 0°C to +70°C, V_{CC} = 5.0V ±10%.

Pin names in parentheses apply to the 80C188EA/80L188EA.

AC SPECIFICATIONS

AC Characteristics—80L186EA13/80L186EA8

Symbol	Parameter	Min	Max	Min	Max	Units	Notes
INPUT CLOCK		**13 MHz**		**8 MHz**			
T_F	CLKIN Frequency	0	26	0	16	MHz	1
T_C	CLKIN Period	38.5	∞	62.5	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	1	8	ns	1, 3
OUTPUT CLOCK							
T_{CD}	CLKIN to CLKOUT Delay	0	45	0	95	ns	1, 4
T	CLKOUT Period		$2*T_C$		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5		(T/2) − 5		ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5		(T/2) − 5		ns	1
T_{PR}	CLKOUT Rise Time	1	12	1	12	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	12	1	12	ns	1, 5
OUTPUT DELAYS							
T_{CHOV1}	ALE, $\overline{LOCK}$	3	27	3	27	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	32	3	32	ns	1, 4, 6, 8
T_{CHOV3}	$\overline{S2:0}$ ($\overline{DEN}$), DT/$\overline{R}$, $\overline{BHE}$ ($\overline{RFSH}$), A19:16	3	30	3	30	ns	1
T_{CLOV1}	$\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT	3	27	3	27	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{INTA1:0}$	3	32	3	35	ns	1, 4, 6
T_{CLOV3}	$\overline{BHE}$ ($\overline{RFSH}$), $\overline{DEN}$, A19:16	3	30	3	30	ns	1, 4, 6
T_{CLOV4}	AD15:0 (A15:8, AD7:0)	3	34	3	35	ns	1, 4, 6
T_{CLOV5}	$\overline{S2:0}$	3	38	3	40	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ ($\overline{RFSH}$), DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	27	0	27	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0 (A15:8, AD7:0)	0	27	0	27	ns	1

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.
11. T_{CHOVS} applies to $\overline{BHE}$ ($\overline{RFSH}$) and A19:16 only after a HOLD release.
12. Pin names in parentheses apply to the 80C188EA/80L188EA.

AC SPECIFICATIONS

AC Characteristics—80L186EA13/80L186EA8

Symbol	Parameter	Min	Max	Min	Max	Units	Notes
SYNCHRONOUS INPUTS		**13 MHz**		**8 MHz**			
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	22		22		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		3		ns	1, 9
T_{CLIS}	AD15:0 (AD7:0), ARDY, SRDY, DRQ1:0	22		22		ns	1, 10
T_{CLIH}	AD15:0 (AD7:0), ARDY, SRDY, DRQ1:0	3		3		ns	1, 10
T_{CLIS}	HOLD	22		22		ns	1, 9
T_{CLIH}	HOLD	3		3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	22		22		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$ ($\overline{RFSH}$), $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper operation.
11. T_{CHOVS} applies to $\overline{BHE}$ ($\overline{RFSH}$) and A19:16 only after a HOLD release.
12. Pin names in parentheses apply to the 80C188EA/80L188EA.

AC SPECIFICATIONS (Continued)

Relative Timings (80C186EA25/20/13, 80L186EA13/8)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{RHLH}	$\overline{RD}$ Rising to ALE Rising	½T − 10		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHDEX}	$\overline{WR}$ Rising to $\overline{DEN}$ Rising	½T − 10		ns	1
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns	5
T_{OVRH}	ONCE ($\overline{UCS}$, $\overline{LCS}$) Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	ONCE ($\overline{UCS}$, $\overline{LCS}$) to $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.
4. Not applicable to latched A2:1. These signals change only on falling T_1.
5. For write cycle followed by read cycle.
6. Operating conditions for 25 MHz are 0°C to +70°C, V_{CC} = 5.0V ±10%.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 8. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

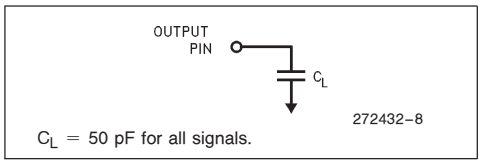


Figure 8. AC Test Load

AC TIMING WAVEFORMS

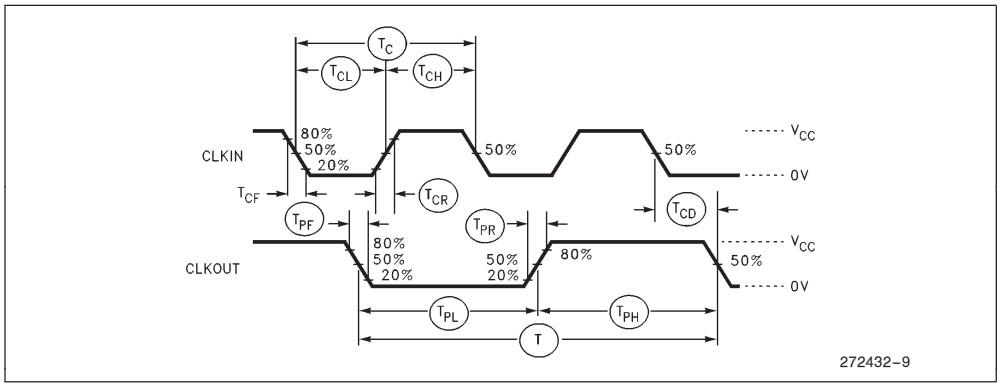
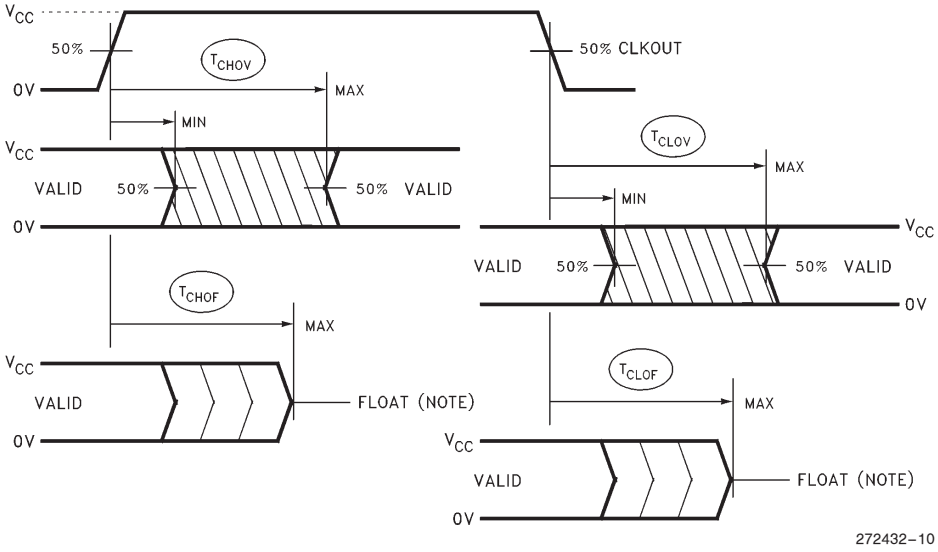
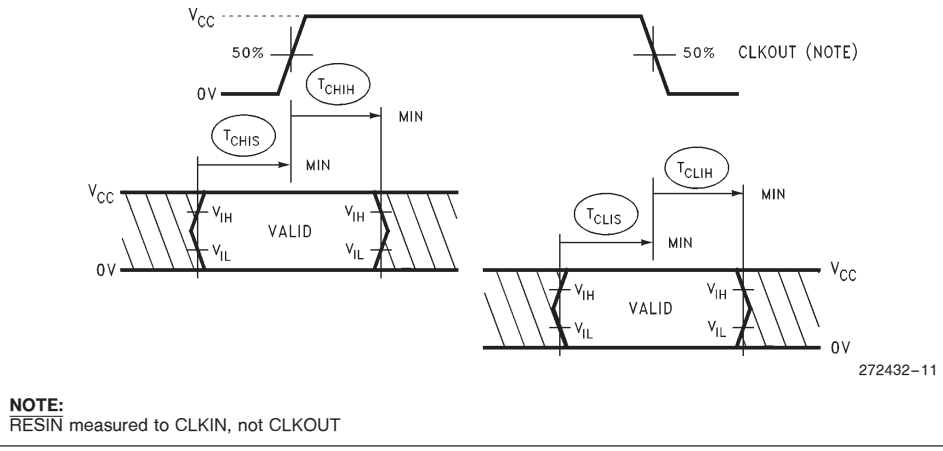


Figure 9. Input and Output Clock Waveform



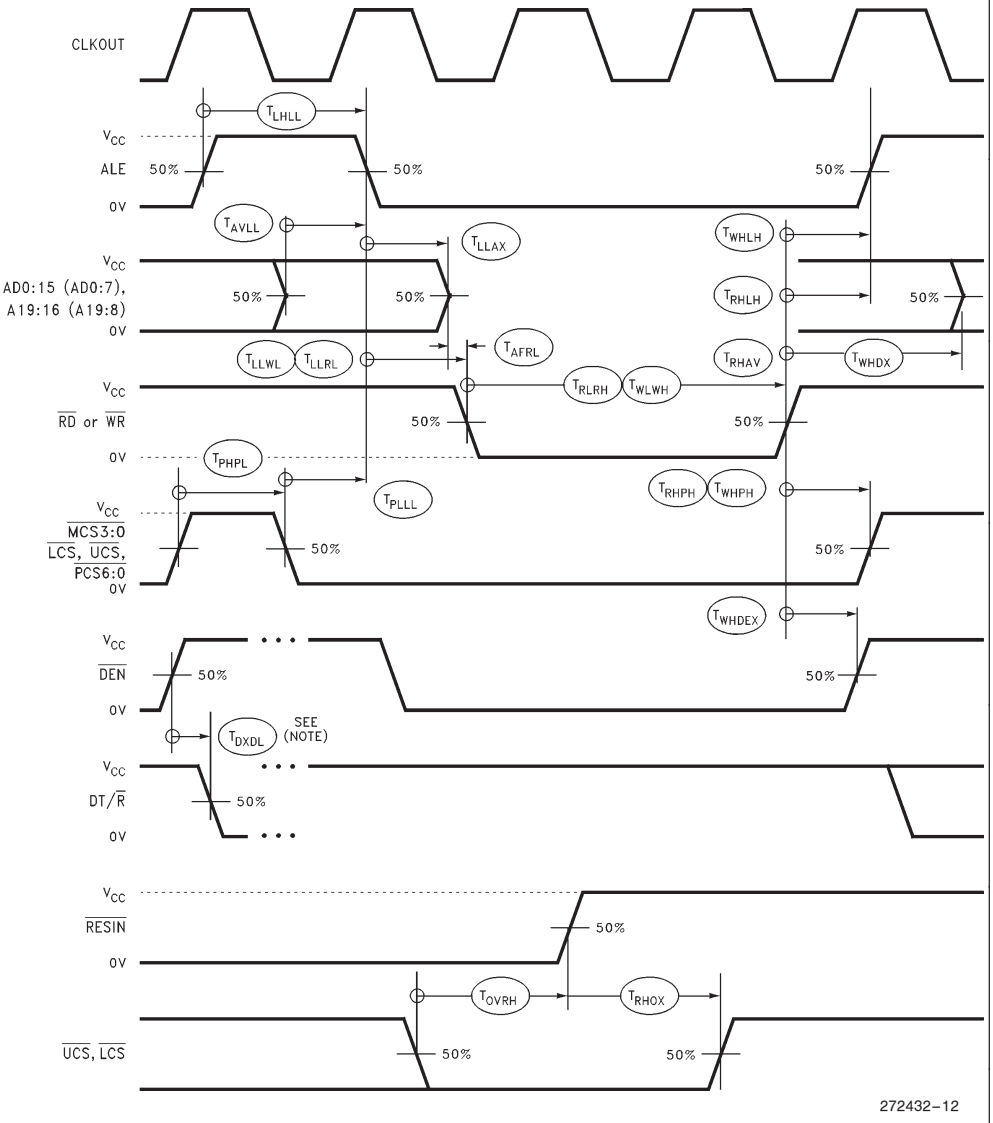
NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 10. Output Delay and Float Waveform



NOTE:
RESIN measured to CLKIN, not CLKOUT

Figure 11. Input Setup and Hold



NOTES:
1. T_{DXDL} for write cycle followed by read cycle.
2. Pin names in parentheses apply to tthe 80C188EA.

Figure 12. Relative Signal Waveform

DERATING CURVES

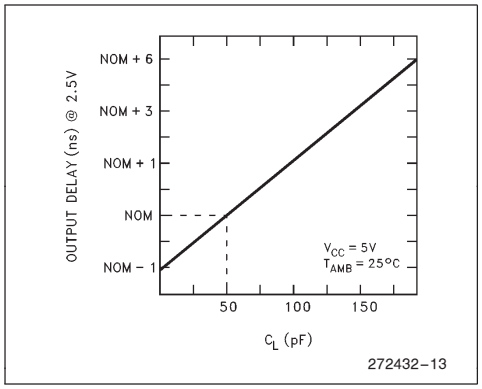


Figure 13. Typical Output Delay Variations Versus Load Capacitance

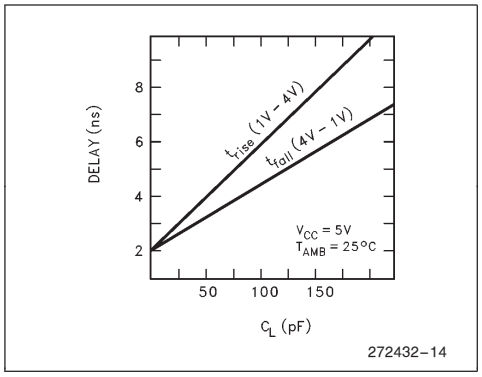


Figure 14. Typical Rise and Fall Variations Versus Load Capacitance

RESET

The processor performs a reset operation any time the $\overline{\text{RESIN}}$ pin is active. The $\overline{\text{RESIN}}$ pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{\text{RESIN}}$ must be held active (low) in order to guarantee correct initialization of the processor. **Failure to provide $\overline{\text{RESIN}}$ while the device is powering up will result in unspecified operation of the device.**

Figure 15 shows the correct reset sequence when first applying power to the processor. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the processor. When attaching a crystal to the device, $\overline{\text{RESIN}}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{\text{RESIN}}$ pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{\text{RESIN}}$ is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 16 shows the timing sequence when $\overline{\text{RESIN}}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the processor to a known operating state. Any bus operation that is in progress at the time $\overline{\text{RESIN}}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{\text{RESIN}}$ is active, signals $\overline{\text{RD}}$/$\overline{\text{QSMD}}$, $\overline{\text{UCS}}$, $\overline{\text{LCS}}$, $\overline{\text{MCS0}}$/PEREQ, $\overline{\text{MCS1}}$/$\overline{\text{ERROR}}$, $\overline{\text{LOCK}}$, and $\overline{\text{TEST}}$/BUSY are configured as inputs and weakly held high by internal pullup transistors. Forcing $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ low selects ONCE Mode. Forcing $\overline{\text{QSMD}}$ low selects Queue Status Mode. Forcing $\overline{\text{TEST}}$/BUSY high at reset and low four clocks later enables Numerics Mode. Forcing $\overline{\text{LOCK}}$ low is prohibited and results in unspecified operation.

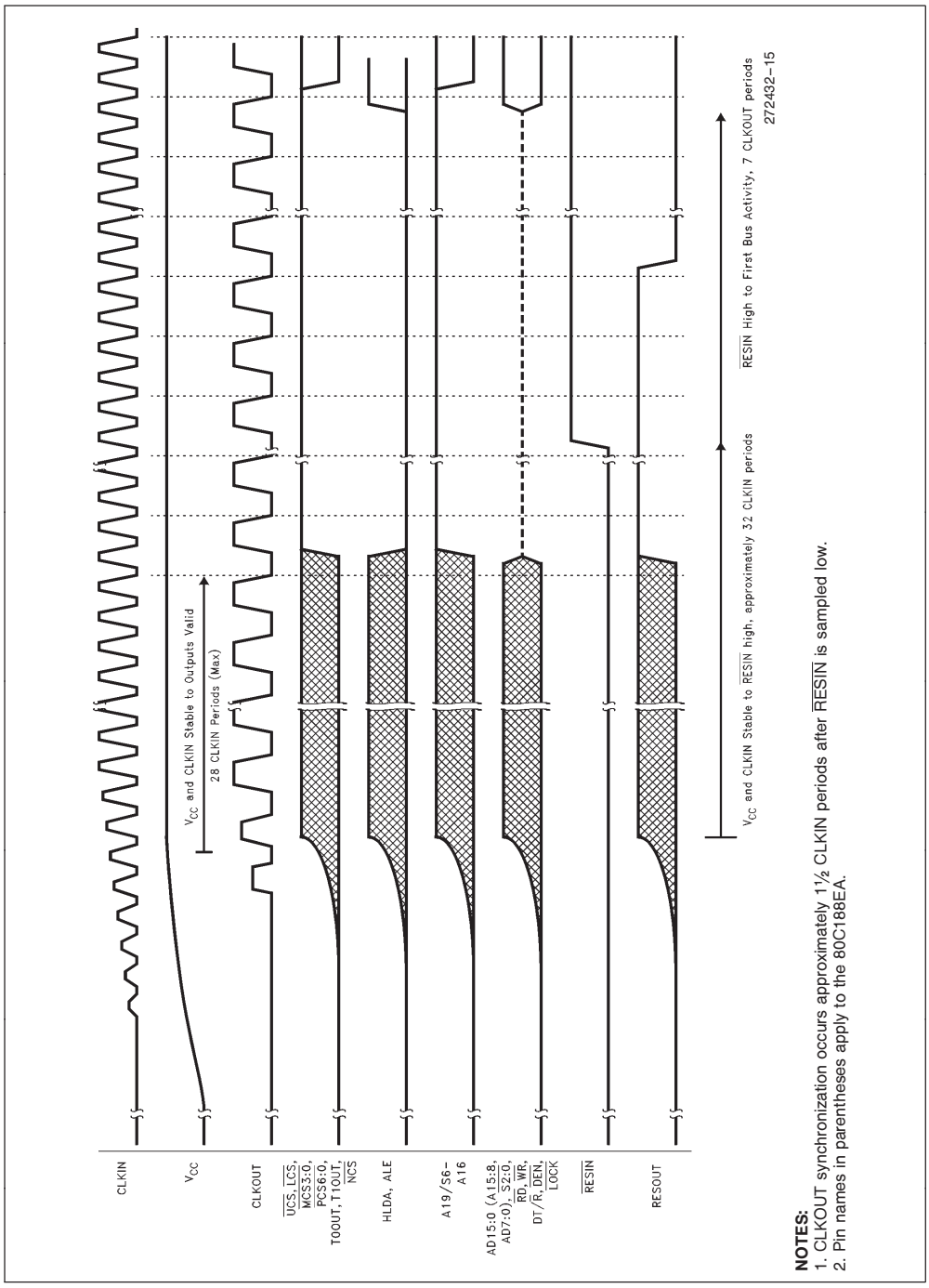


Figure 15. Powerup Reset Waveforms

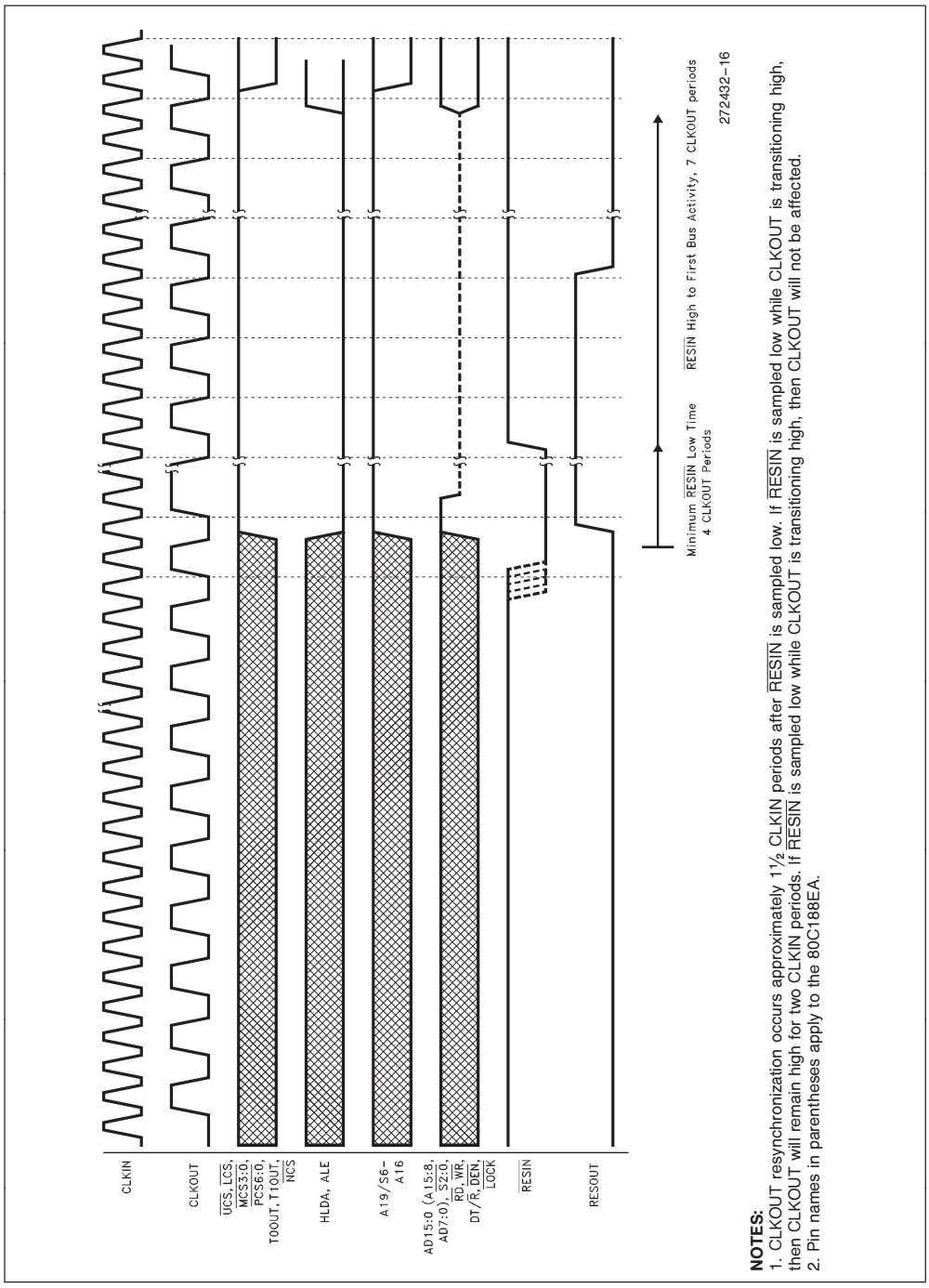
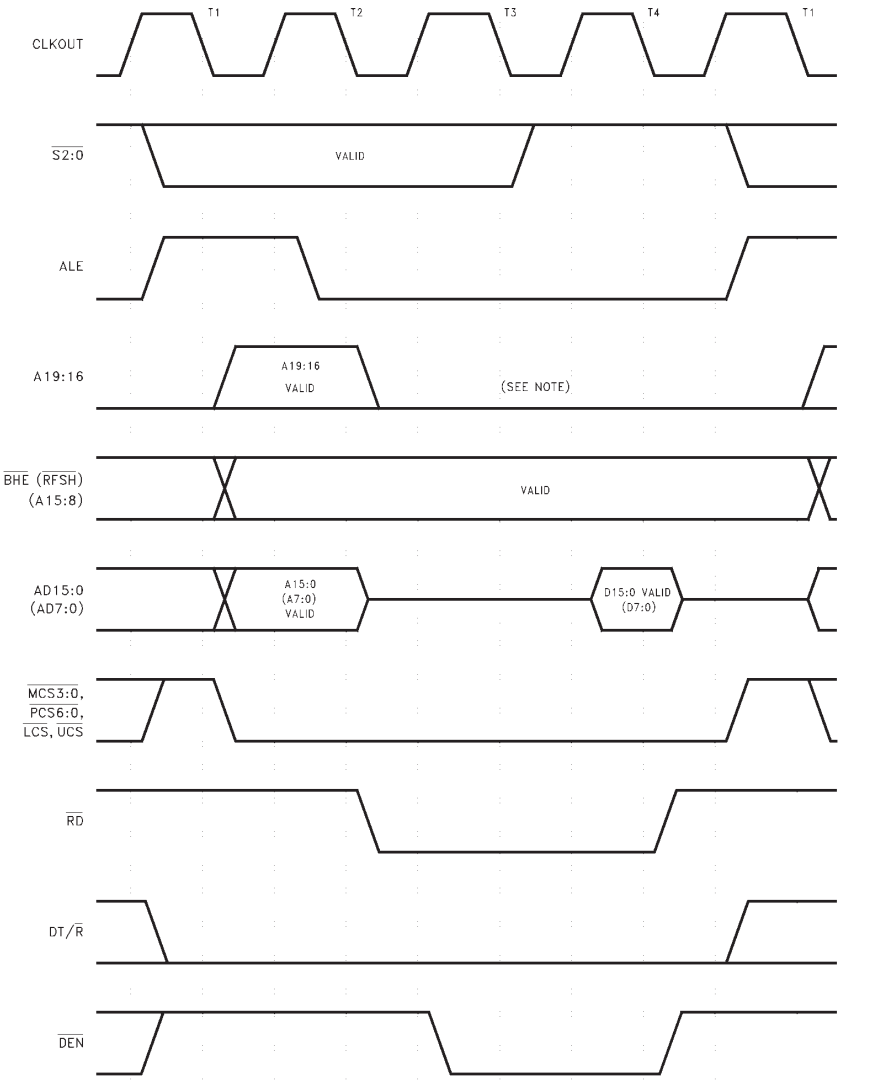


Figure 16. Warm Reset Waveforms

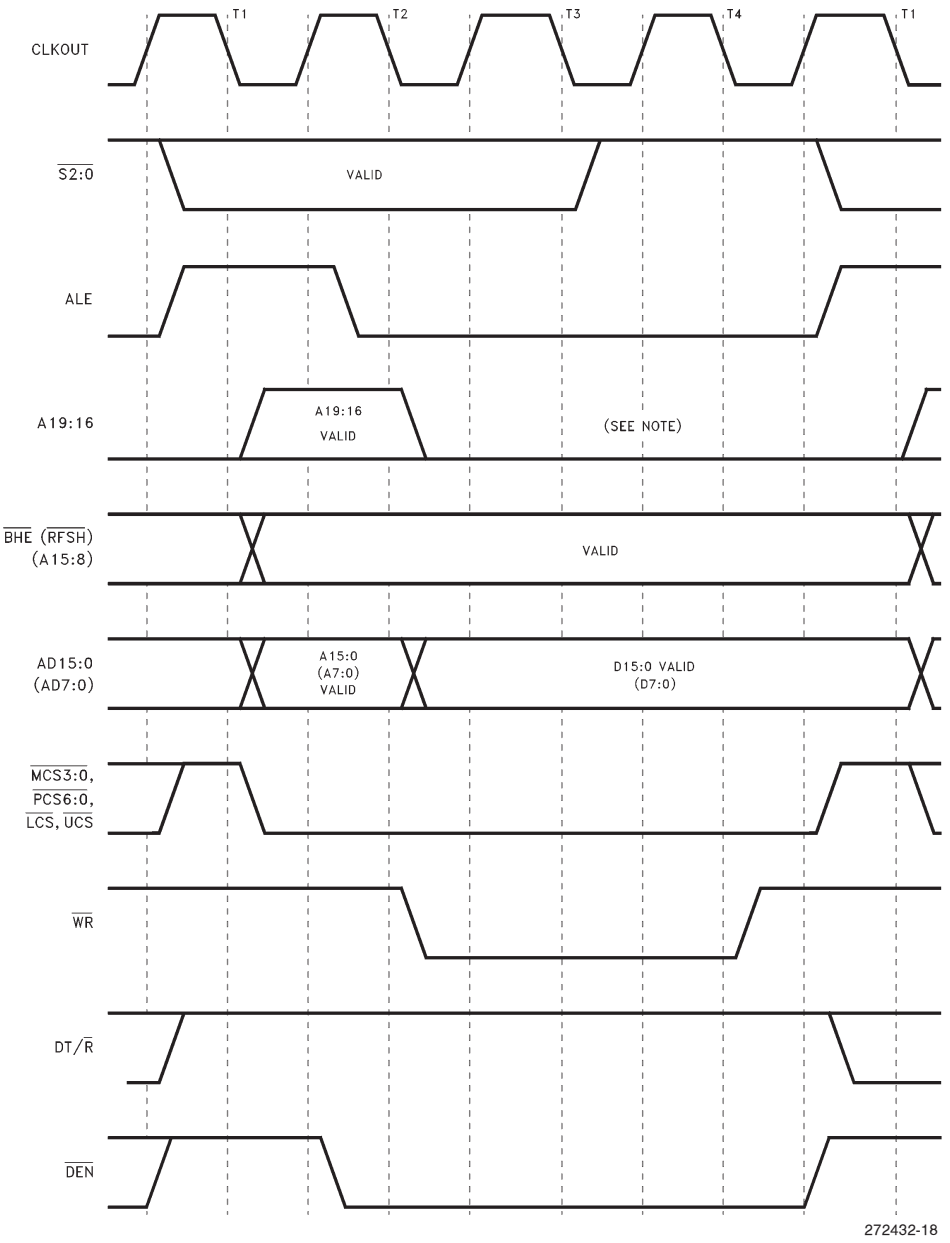
BUS CYCLE WAVEFORMS

Figures 17 through 23 present the various bus cycles that are generated by the processor. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.



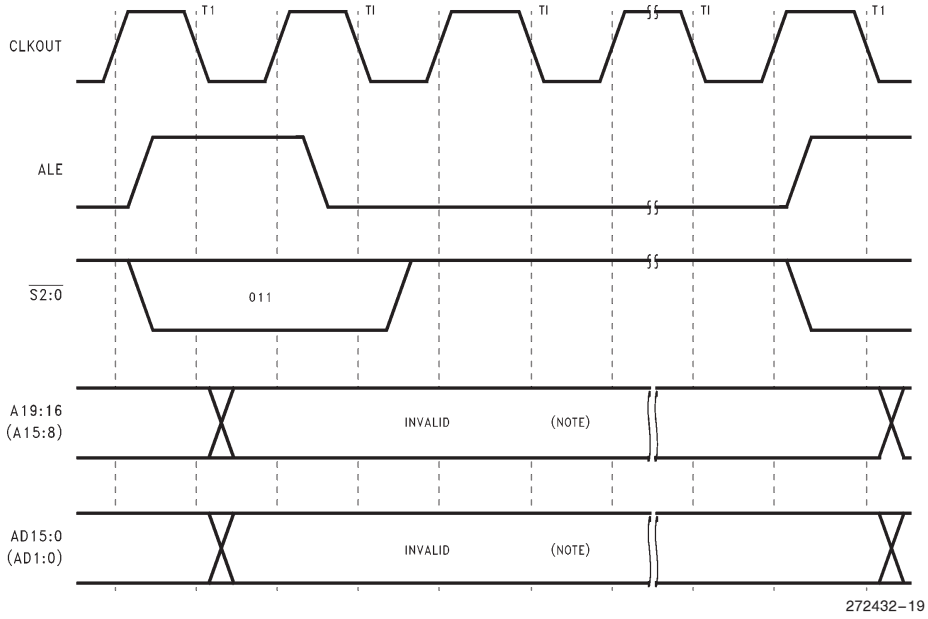
NOTES:
1. During the data phase of the bus cycle, A19/S6 is driven high for a DMA or refresh cycle.
2. Pin names in parentheses apply to the 80C188EA.

Figure 17. Read, Fetch and Refresh Cycle Waveform



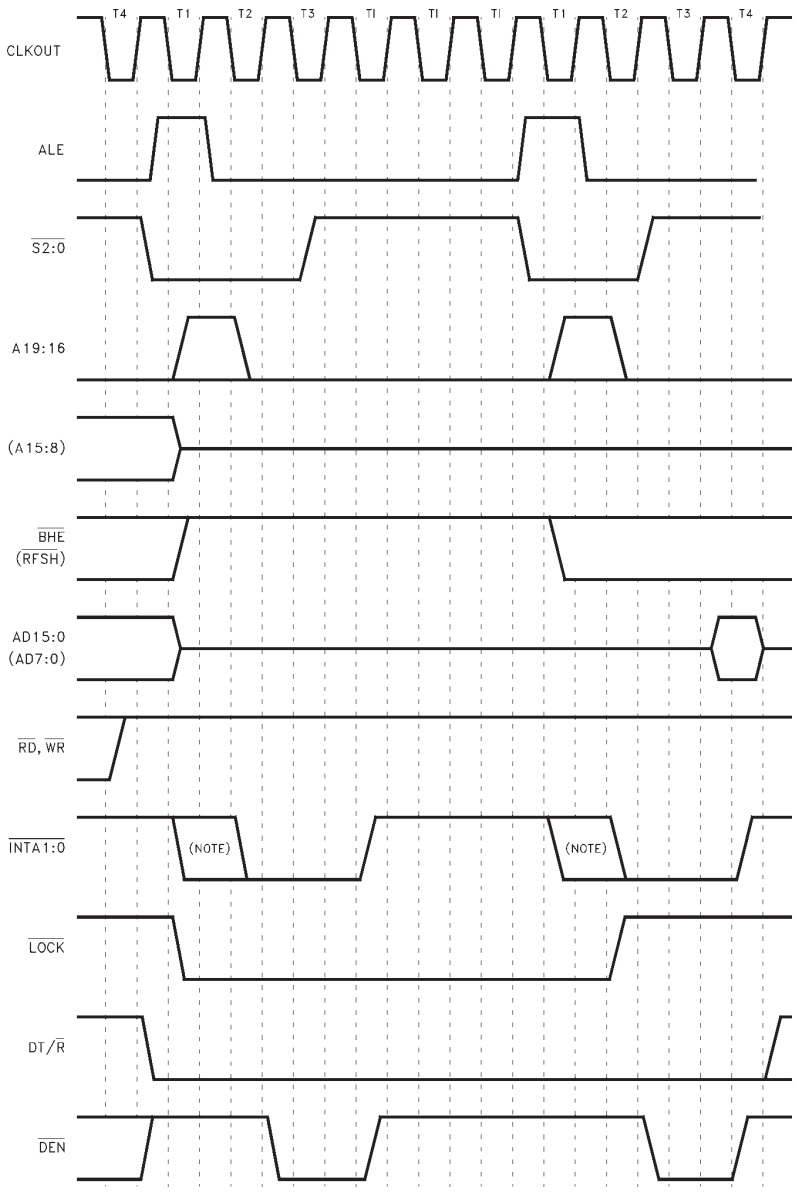
NOTES:
1. During the data phase of the bus cycle, A19/S6 is driven high for a DMA cycle.
2. Pin names in parentheses apply to the 80C188EA.

Figure 18. Write Cycle Waveform



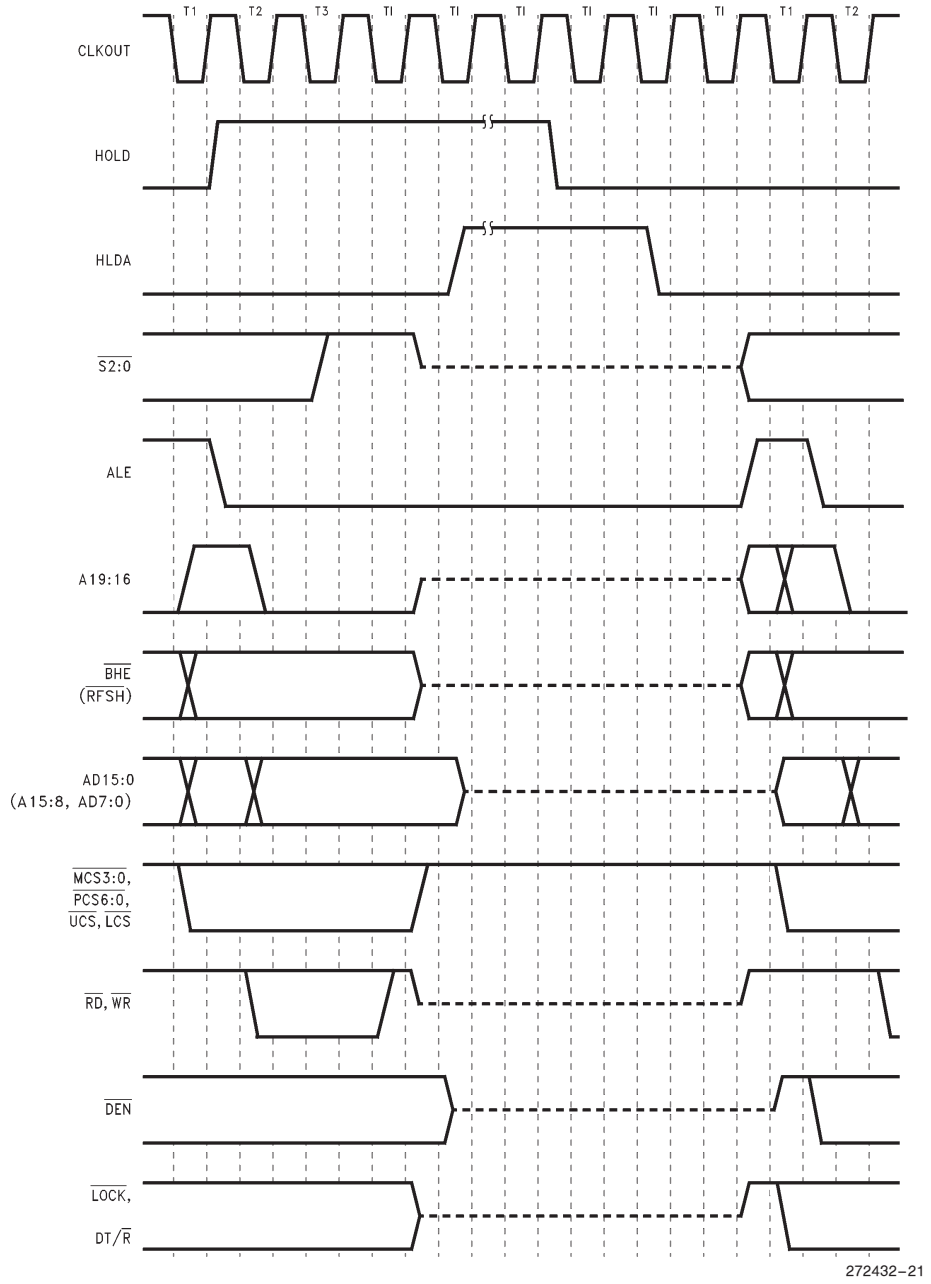
NOTES:
1. The processor drives these pins to 0 during Idle and Powerdown Modes.
2. Pin names in parentheses apply to the 80C188EA.

Figure 19. Halt Cycle Waveform



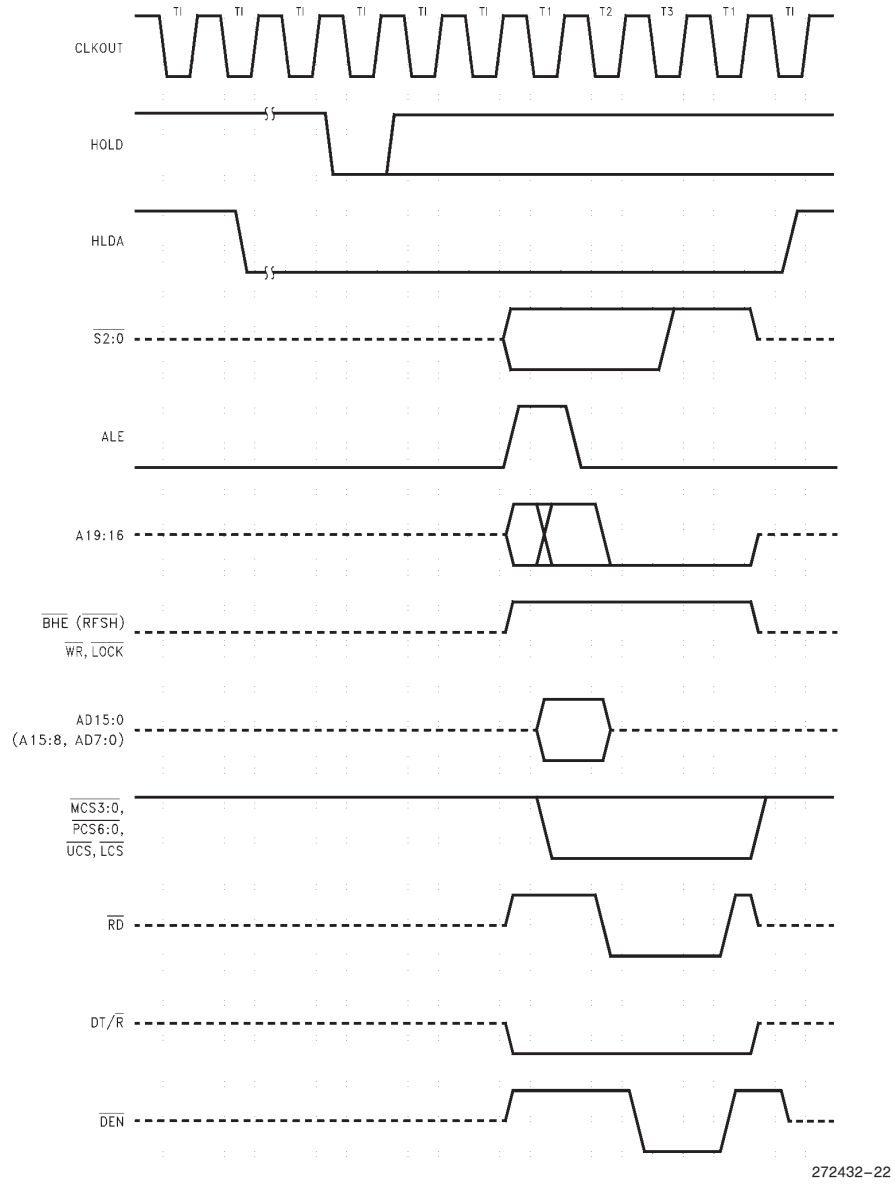
NOTES:
1. INTA occurs one clock later in Slave Mode.
2. Pin names in parentheses apply to the 80C188EA.

Figure 20. INTA Cycle Waveform



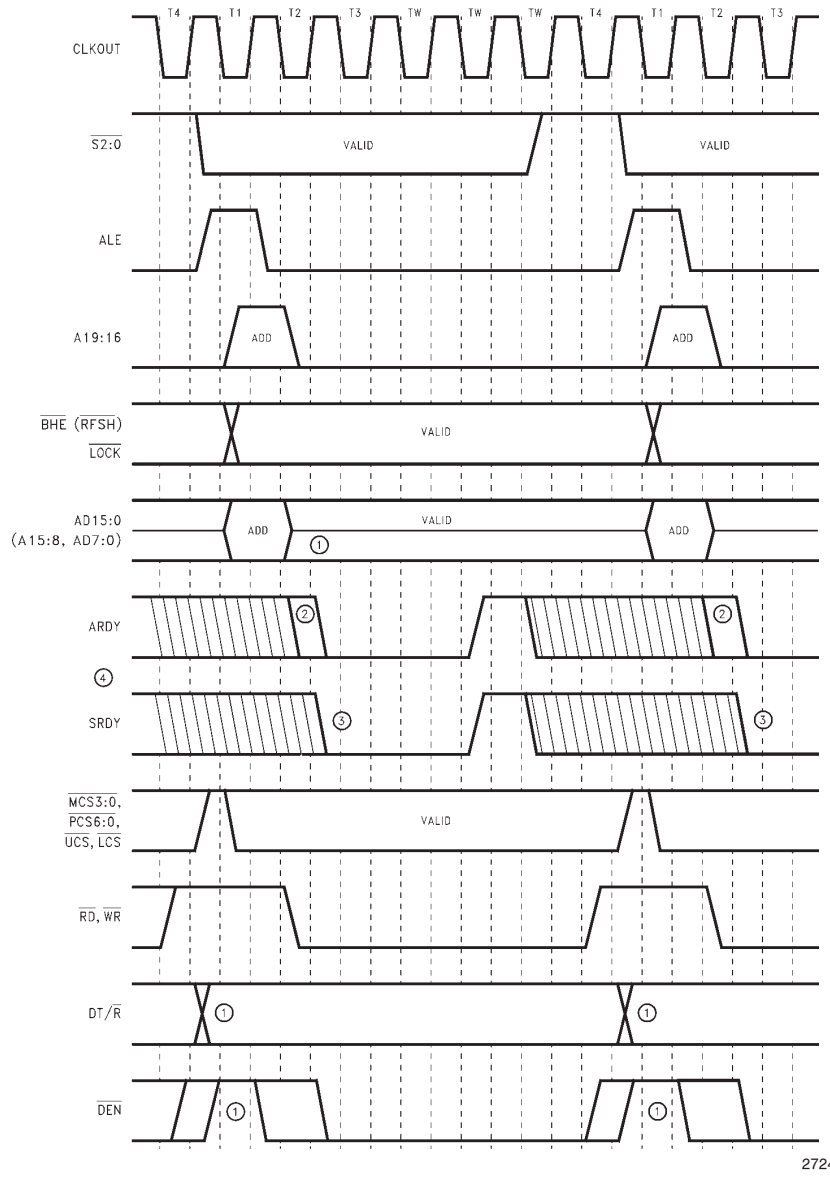
NOTE:
1. Pin names in parentheses apply to the 80C188EA.

Figure 21. HOLD/HLDA Waveform



NOTE:
1. Pin names in parentheses apply to the 80C188EA.

Figure 22. DRAM Refresh Cycle During Hold Acknowledge



NOTES:
1. Generalized diagram for READ or WRITE.
2. ARDY low by either edge causes a wait state. Only rising ARDY is fully synchronized.
3. SRDY low causes a wait state. SRDY must meet setup and hold times to ensure correct device operation.
4. Either ARDY or SRDY active high will terminate a bus cycle.
5. Pin names in parentheses apply to the 80C188EA.

Figure 23. Ready Waveform

80C186EA/80C188EA EXECUTION TIMINGS

A determination of program exeuction timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycle for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries. (80C186EA only)

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186EA has sufficient bus performance to endure that an adequate number of prefetched bytes will reside in the queue (6 bytes) most of the time. Therefore, actual program exeuction time will not be substanially greater than that derived from adding the instruction timings shown.

The 80C188EA 8-bit BIU is limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue (4 bytes) much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				80C186EA Clock Cycles	80C188EA Clock Cycles	Comments
DATA TRANSFER							
MOV = Move:							
Register to Register/Memory	1 0 0 0 1 0 0 w	mod reg r/m			2/12	2/12*	
Register/memory to register	1 0 0 0 1 0 1 w	mod reg r/m			2/9	2/9	
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 000 r/m	data	data if w=1	12–13	12–13	8/16-bit
Immediate to register	1 0 1 1 w reg	data	data if w=1		3–4	3–4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high		8	8*	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high		9	9*	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m			2/9	2/13	
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m			2/11	2/15	
PUSH = Push:							
Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m			16	20	
Register	0 1 0 1 0 reg				10	14	
Segment register	0 0 0 reg 1 1 0				9	13	
Immediate	0 1 1 0 1 0 s 0	data	data if s=0		10	14	
PUSHA = Push All	0 1 1 0 0 0 0 0				36	68	
POP = Pop:							
Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m			20	24	
Register	0 1 0 1 1 reg				10	14	
Segment register	0 0 0 reg 1 1 1	(reg≠01)			8	12	
POPA = Pop All	0 1 1 0 0 0 0 1				51	83	
XCHG = Exchange:							
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m			4/17	4/17*	
Register with accumulator	1 0 0 1 0 reg				3	3	
IN = Input from:							
Fixed port	1 1 1 0 0 1 0 w	port			10	10*	
Variable port	1 1 1 0 1 1 0 w				8	7*	
OUT = Output to:							
Fixed port	1 1 1 0 0 1 1 w	port			9	9*	
Variable port	1 1 1 0 1 1 1 w				7	7*	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1				11	15	
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m			6	6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m	(mod≠11)		18	26	
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m	(mod≠11)		18	26	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1				2	2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0				3	3	
PUSHF = Push flags	1 0 0 1 1 1 0 0				9	13	
POPF = Pop flags	1 0 0 1 1 1 0 1				8	12	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	80C186EA Clock Cycles	80C188EA Clock Cycles	Comments
DATA TRANSFER (Continued)				
SEGMENT = Segment Override:				
CS	0 0 1 0 1 1 1 0	2	2	
SS	0 0 1 1 0 1 1 0	2	2	
DS	0 0 1 1 1 1 1 0	2	2	
ES	0 0 1 0 0 1 1 0	2	2	
ARITHMETIC				
ADD = Add:				
Reg/memory with register to either	0 0 0 0 0 0 d w | mod reg r/m	3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 0 0 r/m | data | data if s w = 01	4/16	4/16*	
Immediate to accumulator	0 0 0 0 0 1 0 w | data | data if w = 1	3/4	3/4	8/16-bit
ADC = Add with carry:				
Reg/memory with register to either	0 0 0 1 0 0 d w | mod reg r/m	3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 1 0 r/m | data | data if s w = 01	4/16	4/16*	
Immediate to accumulator	0 0 0 1 0 1 0 w | data | data if w = 1	3/4	3/4	8/16-bit
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 0 r/m	3/15	3/15*	
Register	0 1 0 0 0 reg	3	3	
SUB = Subtract:				
Reg/memory and register to either	0 0 1 0 1 0 d w | mod reg r/m	3/10	3/10*	
Immediate from register/memory	1 0 0 0 0 0 s w | mod 1 0 1 r/m | data | data if s w = 01	4/16	4/16*	
Immediate from accumulator	0 0 1 0 1 1 0 w | data | data if w = 1	3/4	3/4	8/16-bit
SBB = Subtract with borrow:				
Reg/memory and register to either	0 0 0 1 1 0 d w | mod reg r/m	3/10	3/10*	
Immediate from register/memory	1 0 0 0 0 0 s w | mod 0 1 1 r/m | data | data if s w = 01	4/16	4/16*	
Immediate from accumulator	0 0 0 1 1 1 0 w | data | data if w = 1	3/4	3/4*	8/16-bit
DEC = Decrement				
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	3/15	3/15*	
Register	0 1 0 0 1 reg	3	3	
CMP = Compare:				
Register/memory with register	0 0 1 1 1 0 1 w | mod reg r/m	3/10	3/10*	
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	3/10	3/10*	
Immediate with register/memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w = 01	3/10	3/10*	
Immediate with accumulator	0 0 1 1 1 1 0 w | data | data if w = 1	3/4	3/4	8/16-bit
NEG = Change sign register/memory	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	3/10*	3/10*	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	4	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 100 r/m			
Register-Byte		26–28	26–28	
Register-Word		35–37	35–37	
Memory-Byte		32–34	32–34	
Memory-Word		41–43	41–48*	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				80C186EA Clock Cycles	80C188EA Clock Cycles	Comments
ARITHMETIC (Continued)							
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w	mod 1 0 1 r/m					
Register-Byte					25–28	25–28	
Register-Word					34–37	34–37	
Memory-Byte					31–34	32–34	
Memory-Word					40–43	40–43*	
IMUL = Integer Immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s=0	22–25 29–32	22-25 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 1 1 0 r/m					
Register-Byte					29	29	
Register-Word					38	38	
Memory-Byte					35	35	
Memory-Word					44	44*	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 1 1 1 r/m					
Register-Byte					44–52	44–52	
Register-Word					53–61	53–61	
Memory-Byte					50–58	50–58	
Memory-Word					59–67	59–67*	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	4	
LOGIC **Shift/Rotate Instructions:**							
Register/Memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15	2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n	5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n	5+n/17+n	
	TTT Instruction 0 0 0 ROL 0 0 1 ROR 0 1 0 RCL 0 1 1 RCR 1 0 0 SHL/SAL 1 0 1 SHR 1 1 1 SAR						
AND = **And:**							
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1	4/16	4/16*	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1		3/4	3/4*	8/16-bit
TEST=**And function to flags, no result:**							
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	3/10*	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1	4/10	4/10*	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1		3/4	3/4	8/16-bit
OR=**Or:**							
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1	4/16	4/16*	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1		3/4	3/4*	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	80C186EA Clock Cycles	80C188EA Clock Cycles	Comments
LOGIC (Continued)				
XOR = **Exclusive or:**				
Reg/memory and register to either	0 0 1 1 0 0 d w | mod reg r/m	3/10	3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w=1	4/16	4/16*	
Immediate to accumulator	0 0 1 1 0 1 0 w | data | data if w=1	3/4	3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w | mod 0 1 0 r/m	3/10	3/10*	
STRING MANIPULATION				
MOVS = Move byte/word	1 0 1 0 0 1 0 w	14	14*	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w	22	22*	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w	15	15*	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w	12	12*	
STOS = Store byte/wd from AL/AX	1 0 1 0 1 0 1 w	10	10*	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w	14	14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w	14	14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)				
MOVS = Move string	1 1 1 1 0 0 1 0 | 1 0 1 0 0 1 0 w	8+8n	8+8n*	
CMPS = Compare string	1 1 1 1 0 0 1 z | 1 0 1 0 0 1 1 w	5+22n	5+22n	
SCAS = Scan string	1 1 1 1 0 0 1 z | 1 0 1 0 1 1 1 w	5+15n	5+15n*	
LODS = Load string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 1 0 w	6+11n	6+11n*	
STOS = Store string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 0 1 w	6+9n	6+9n*	
INS = Input string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 0 w	8+8n	8+8n*	
OUTS = Output string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 1 w	8+8n	8+8n*	
CONTROL TRANSFER				
CALL = **Call:**				
Direct within segment	1 1 1 0 1 0 0 0 | disp-low | disp-high	15	19	
Register/memory indirect within segment	1 1 1 1 1 1 1 1 | mod 0 1 0 r/m	13/19	17/27	
Direct intersegment	1 0 0 1 1 0 1 0 | segment offset | segment selector	23	31	
Indirect intersegment	1 1 1 1 1 1 1 1 | mod 0 1 1 r/m (mod ≠ 11)	38	54	
JMP = **Unconditional jump:**				
Short/long	1 1 1 0 1 0 1 1 | disp-low	14	14	
Direct within segment	1 1 1 0 1 0 0 1 | disp-low | disp-high	14	14	
Register/memory indirect within segment	1 1 1 1 1 1 1 1 | mod 1 0 0 r/m	11/17	11/21	
Direct intersegment	1 1 1 0 1 0 1 0 | segment offset | segment selector	14	14	
Indirect intersegment	1 1 1 1 1 1 1 1 | mod 1 0 1 r/m (mod ≠ 11)	26	34	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	80C186EA Clock Cycles	80C188EA Clock Cycles	Comments
CONTROL TRANSFER (Continued)				
RET = **Return from CALL:**				
Within segment	11000011	16	20	
Within seg adding immed to SP	11000010 data-low data-high	18	22	
Intersegment	11001011	22	30	
Intersegment adding immediate to SP	11001010 data-low data-high	25	33	
JE/JZ = Jump on equal/zero	01110100 disp	4/13	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100 disp	4/13	4/13	
JLE/JNG = Jump on less or equal/not greater	01111110 disp	4/13	4/13	
JB/JNAE = Jump on below/not above or equal	01110010 disp	4/13	4/13	
JBE/JNA = Jump on below or equal/not above	01110110 disp	4/13	4/13	
JP/JPE = Jump on parity/parity even	01111010 disp	4/13	4/13	
JO = Jump on overflow	01110 000 disp	4/13	4/13	
JS = Jump on sign	01111000 disp	4/13	4/13	
JNE/JNZ = Jump on not equal/not zero	01110101 disp	4/13	4/13	
JNL/JGE = Jump on not less/greater or equal	01111101 disp	4/13	4/13	
JNLE/JG = Jump on not less or equal/greater	01111111 disp	4/13	4/13	
JNB/JAE = Jump on not below/above or equal	01110011 disp	4/13	4/13	
JNBE/JA = Jump on not below or equal/above	01110111 disp	4/13	4/13	
JNP/JPO = Jump on not par/par odd	01111011 disp	4/13	4/13	
JNO = Jump on not overflow	01110001 disp	4/13	4/13	
JNS = Jump on not sign	01111001 disp	4/13	4/13	
JCXZ = Jump on CX zero	11100011 disp	5/15	5/15	
LOOP = Loop CX times	11100010 disp	6/16	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001 disp	6/16	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000 disp	6/16	6/16	
ENTER = Enter Procedure	11001000 data-low data-high L			
L = 0		15	19	
L = 1		25	29	
L > 1		22+16(n−1)	26+20(n−1)	
LEAVE = Leave Procedure	11001001	8	8	
INT = **Interrupt:**				
Type specified	11001101 type	47	47	
Type 3	11001100	45	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110	48/4	48/4	
IRET = Interrupt return	11001111	28	28	
BOUND = Detect value out of range	01100010 mod reg r/m	33–35	33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	80C186EA Clock Cycles	80C188EA Clock Cycles	Comments
PROCESSOR CONTROL				
CLC = Clear carry	11111000	2	2	
CMC = Complement carry	11110101	2	2	
STC = Set carry	11111001	2	2	
CLD = Clear direction	11111100	2	2	
STD = Set direction	11111101	2	2	
CLI = Clear interrupt	11111010	2	2	
STI = Set interrupt	11111011	2	2	
HLT = Halt	11110100	2	2	
WAIT = Wait	10011011	6	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	2	
NOP = No Operation	10010000 (TTT LLL are opcode to processor extension)	3	3	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word operations, add 4 clock cycles for all memory transfers.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

Intel 80C186EA/80L186EA devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet update is valid for devices with an ''A'', ''B'', ''C'', ''D'', or ''E'' as the ninth character in the FPO number, as illustrated in Figure 5 for the 68-lead PLCC package, Figure 6 for the 84-lead QFP (EIAJ) package, and Figure 7 for the 80-lead SQFP device. Such devices may also be identified by reading a value of 01H, 02H, 03H from the STEPID register.

This data sheet replaces the following data sheets:

272019-002—80C186EA
272020-002—80C188EA
272021-002—80L186EA
272022-002—80L188EA
272307-001—SB80C186EA/SB80L186EA
272308-001—SB80C188EA/SB80L188EA

ERRATA

An 80C186EA/80L186EA with a STEPID value of 01H or 02H has the following known errata. A device with a STEPID of 01H or 02H can be visually identified by noting the presence of an ''A'', ''B'', or ''C'' alpha character, next to the FPO number. The FPO number location is shown in Figures 5, 6, and 7.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

An 80C186EA/80L186EA with a STEPID value of 03H has no known errata. A device with a STEPID of 03H can be visually identified by noting the presence of a ''D'' or ''E'' alpha character next to the FPO number. The FPO number location is shown in Figures 5, 6, and 7.