

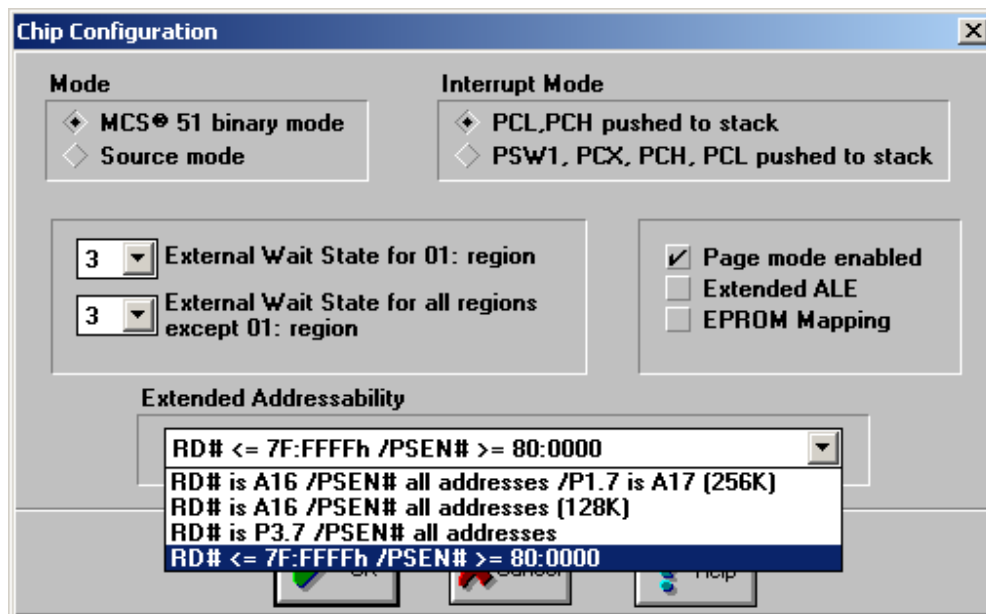
DS-251 Setup

Depending on Configuration Registers, 8xC251 processors are supported in 4 operation modes:

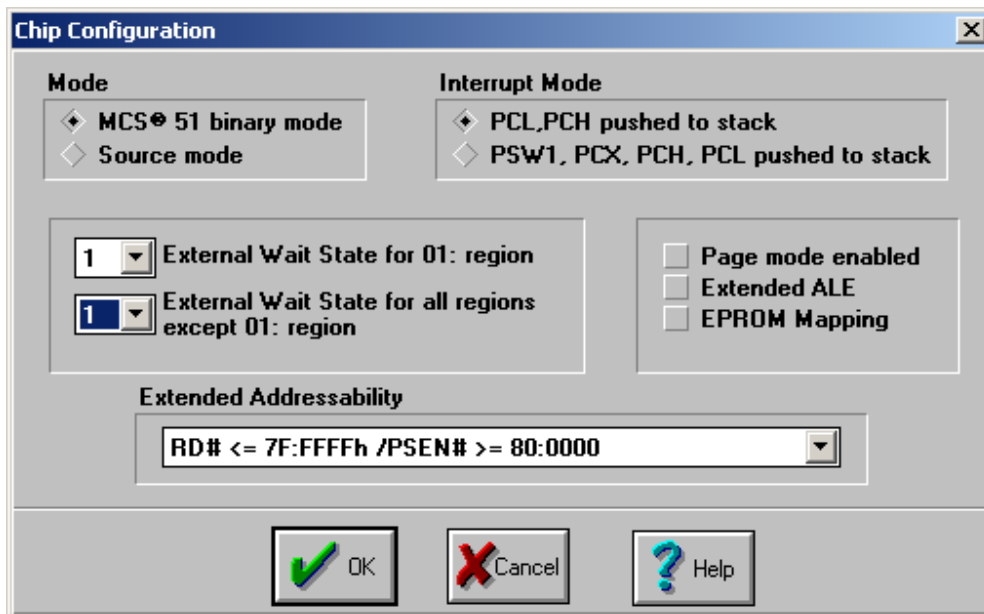
Table 7. Memory Signal Selections (RD1:0)

RD1:0	P1.7/CEX/ A17/WCLK	P3.7/RD#/A16	PSEN#	WR#	Features
0 0	A17	A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external memory
0 1	P1.7/CEX4/ WCLK	A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external memory
1 0	P1.7/CEX4/ WCLK	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	64-Kbyte external memory. One additional port pin.
1 1	P1.7/CEX4/ WCLK	RD# asserted for addresses $\leq 7F:FFFFH$	Asserted for $\geq 80:0000H$	Asserted only for writes to MCS 51 microcontroller data memory locations.	64-Kbyte external memory. Compatible with MCS 51 micro-controllers.

These modes are selectable in Options/Architecture/Chip configuration mode of CEIBO Windows debugger.



Typical configuration for **8051 compatible mode**:



The 'Chip Configuration' dialog box for 8051 compatible mode features a blue title bar with a close button. It is divided into several sections: 'Mode' with radio buttons for 'MCS-51 binary mode' (selected) and 'Source mode'; 'Interrupt Mode' with radio buttons for 'PCL,PCH pushed to stack' (selected) and 'PSW1, PCX, PCH, PCL pushed to stack'; two dropdown menus for 'External Wait State' (both set to '1'); a group of unchecked checkboxes for 'Page mode enabled', 'Extended ALE', and 'EPROM Mapping'; and an 'Extended Addressability' section with a text box showing 'RD# <= 7F:FFFFh /PSEN# >= 80:0000'. At the bottom are three buttons: 'OK' with a green checkmark, 'Cancel' with a red X, and 'Help' with a blue question mark.

Chip Configuration

Mode

- ☒ MCS-51 binary mode
- ☐ Source mode

Interrupt Mode

- ☒ PCL,PCH pushed to stack
- ☐ PSW1, PCX, PCH, PCL pushed to stack

External Wait State for 01: region: 1

External Wait State for all regions except 01: region: 1

Page mode enabled ☐

Extended ALE ☐

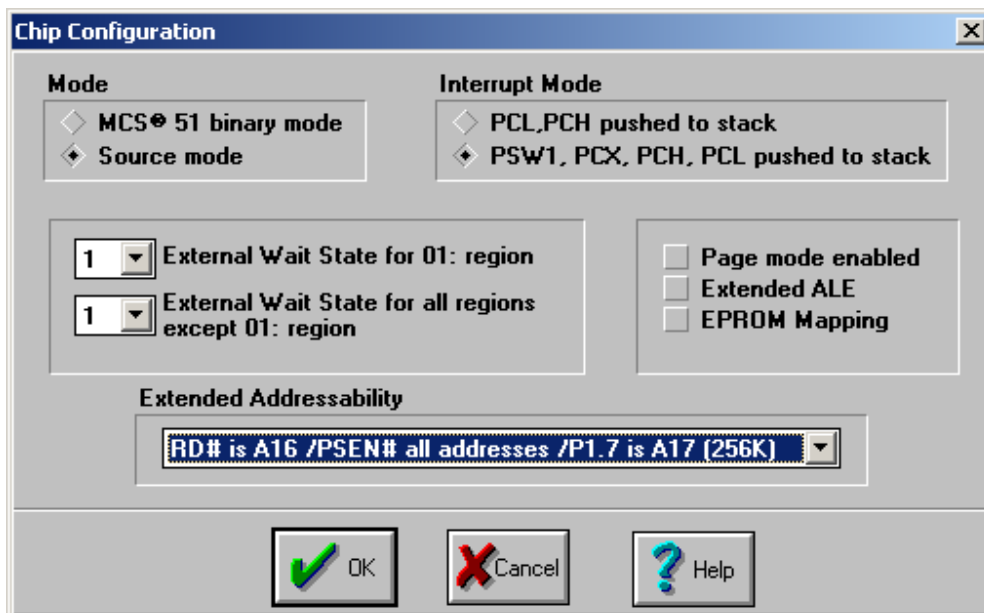
EPROM Mapping ☐

Extended Addressability

RD# <= 7F:FFFFh /PSEN# >= 80:0000

OK Cancel Help

Typical configuration for **80251 Source mode**:



The 'Chip Configuration' dialog box for 80251 Source mode has a similar layout to the 8051 version. In the 'Mode' section, 'Source mode' is selected. In the 'Interrupt Mode' section, 'PSW1, PCX, PCH, PCL pushed to stack' is selected. The 'Extended Addressability' text box shows 'RD# is A16 /PSEN# all addresses /P1.7 is A17 (256K)'. The 'OK', 'Cancel', and 'Help' buttons are at the bottom.

Chip Configuration

Mode

- ☐ MCS-51 binary mode
- ☒ Source mode

Interrupt Mode

- ☐ PCL,PCH pushed to stack
- ☒ PSW1, PCX, PCH, PCL pushed to stack

External Wait State for 01: region: 1

External Wait State for all regions except 01: region: 1

Page mode enabled ☐

Extended ALE ☐

EPROM Mapping ☐

Extended Addressability

RD# is A16 /PSEN# all addresses /P1.7 is A17 (256K)

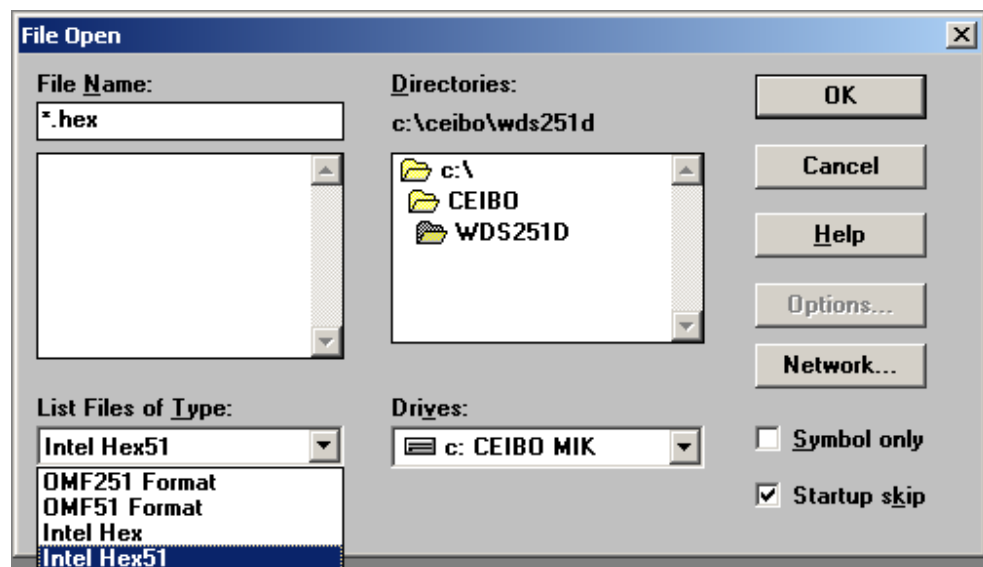
OK Cancel Help

80C251 and 8051 memory map settings are different:

Table 8. 8xC251TA/TB/TP/TQ Address Map

Internal Address)	Description	Notes
FF:FFFFH FF:4000H	External Memory except the top eight bytes (FF:FFF8H–FF:FFFFH) which are reserved for the configuration array.	1, 3, 10
FF:3FFFH FF:0000H	External memory or on-chip nonvolatile memory (8Kbytes FF:0000H - FF:1FFFH, 16Kbytes FF:0000H - FF:3FFFH).	3, 4, 5
FE:FFFFH FE:0000H	External Memory	3
FD:FFFFH 02:0000H	Reserved	6
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:E000H	External memory or with configuration bit EMAP# = 0, addresses in this range access on-chip code memory in region FF: (16 Kbyte devices only).	5, 7
00:DFFFH 00:0420H	External Memory	7
00:041FH 00:0080H	On-chip RAM (512 bytes 00:0020H - 00:021FH, 1024 bytes 00:0020H - 00:041FH)	7
00:007FH 00:0020H	On-chip RAM	8
00:001FH 00:0000H	Storage for R0–R7 of Register File	2, 9

Your **compiler** may generate **output files** in four different formats (two OMF and two HEX formats):



File-Open dialog of CEIBO Windows debugger supports extended OMF (**OMF251**), extended HEX (**Intel HEX**), **OMF51** and **HEX51**. Extended means > 64K which is used for 251 configurations; 8051 configurations are limited to 64K.

According to the above Address Map options (Table 8), code address range of 80C251 is (0FE:0000-0FF:FFFF), while for 8051 is limited to 64K (0-FFFF).

Extended HEX format generated by the compiler supports 251 full address range of the instructions (for example C0FF:0000 LJMP 0500h).

The same instruction address for HEX51 is C0000 LJMP 0500h. This is to support 8051 settings, which is limited to 64K.

Loading HEX51 and OMF51 files starts at 0FF:0000.

Loading Intel HEX and OMF251 according to the addresses defined by your linker.

If you compiled the files to run on an 8051 chip (even if you actually uses a 251) and the generated output is in 80C51 hex or OMF51 format, please select HEX51 or OMF51 in the load dialog **before** loading your code into DS-251. In that case, you can find the loaded program in CPU Window at CFF:0000.

If you use extended HEX or OMF251, select Intel HEX or OMF251 **before** loading your code into DS-251.

If you loaded an HEX51 file but in **List Files of Type** the selection is **wrongly** Intel HEX, your program has been loaded into DATA at address 00:0000 and can not be executed.